Compal Confidential

Nano 110

DIS M/B Schematics Document

Intel Skylake / Kabylake U Processor with DDR4

AMD R17M-M1-70

2016-12-05

LA-D562P

REV :2.0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: Cover Page

Size: C	Document Number: LA-D562P		Rev: 2.0
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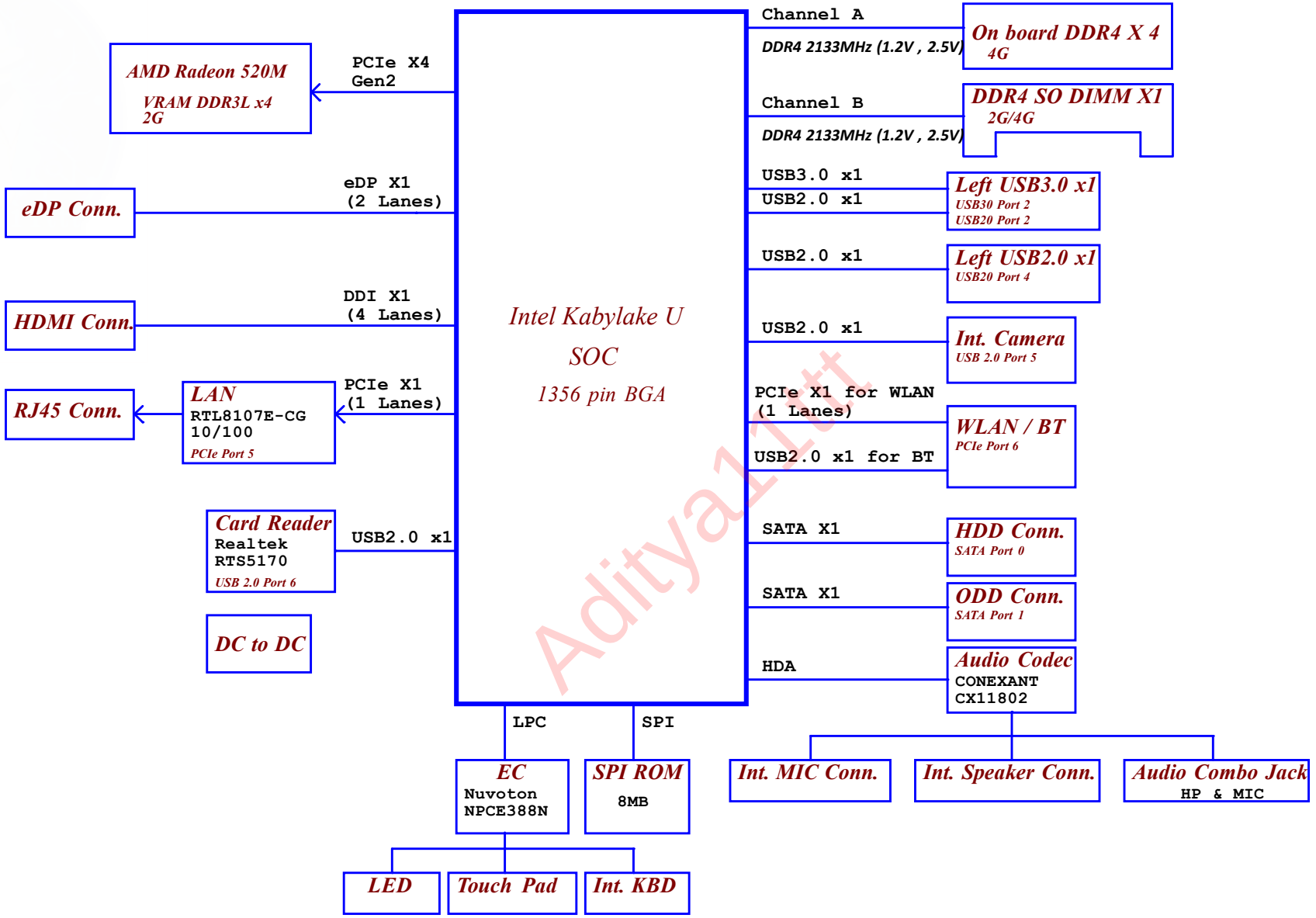

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: Block Diagram
Size: C	Document Number: LA-D562P		Rev: 2.0
Date: Monday, April 10, 2017	Sheet 2 of 52		

Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.2V	+5VS +3VS +1.35VGS +VCCSA +VCCCORE +VCCGT +VGACORE +1.8VS +0.6VS +1VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

PCH SM Bus address

Device	Address	
DDR_JDIMM1	1010 000x	A0h

SMBUS Control Table

	SOURCE	GPU	BATT	NECP388	SODIMM	SOC
SMB_EC_CK1 SMB_EC_DA1	NECP388 +3VALW	X	V +3VALW	X	X	X
SMB_EC_CK2 SMB_EC_DA2	NECP388 +3VS	V +3VGS	X	X	X	V +3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	V +3VS	X
PCH_SML0CLK PCH_SML0DATA	PCH +3VALW	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VGS	X	V +3VS	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V(RAM)	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0		
		1	USB Port (Left Side) USB3.0
	UHCI1	2	
		3	
	UHCI2	4	USB Port (Left Side) USB2.0
		5	Camera
	UHCI3	6	Card Reader
		7	NGFF(WLAN)

USB 3.0 Port Table

Port	
1	
2	USB3 MB(JUSB1)
3	
4	
5	
6	

SATA Port Table

Port	
0	HDD
1	ODD

PCIE Port Table

Port	Lane	
1	1	GPU
2	2	
3	3	
4	4	
5		LAN
6		NGFF WLAN+BT
7		
8		
9		
10		

BOM Structure Table

Item	BOM Structure
CIWP0 (14")	14@
CIWP1 (15")	15@
GPU R16M-M1-30	M1@
GPU R17M-M1-70	M2@
For DIS	PX@
For UMA	UMA@
Camera	CMOS@
EMI pop	EMI@
EMI Un-pop	@EMI@
ESD pop	ESD@
ESD Un-pop	@ESD@
RF pop	RF@
RF unpop	@RF@
R-Short	RS@
Test Point	TP@
VRAM indentify	X76@
System RAM indentify	X76RAM@
HDMI Royalty	45@
Connector	ME@
SA000092P60	CPU1@
SA000092OA0	CPU2@
SA000094250	CPU3@
SA000093780	CPU4@
SA00009QZ10	CPU5@
SA00009QX10	CPU6@
SA0000ACL40	CPU7@
SA0000A3430	CPU8@
SA0000A3730	CPU9@
SA0000A3870	CPU10@
X7667538L01	S4G@
X7667538L02	M4G@
X7667538L06	M4G2@
X7672938L04	S4G2@
X7672938L05	H4G@
X7667538L03	JS2G@
X7667538L04	JM2G@
X7667538L05	JH2G@

UC1 CPU1@ CPU i7 6500U SA000092P60
UC1 CPU2@ CPU i5 6200U SA000092OA0
UC1 CPU3@ CPU 4405U SA000094250
UC1 CPU4@ CPU 3855U SA000093780
UC1 CPU5@ CPU i5 6198DU SA00009QZ10
UC1 CPU6@ CPU i7 6498DU SA00009QX10
UC1 CPU7@ CPU i3-6006U SA0000ACL40
UC1 CPU8@ CPU i7-7500U SA0000A3430
UC1 CPU9@ CPU i5-7200U SA0000A3730
UC1 CPU10@ CPU i3-7100U SA0000A3870
ZZZ 14@ PCB DA6001KC320
ZZZ 15@ PCB DA6001KC220
UV1 M1@ VGA SA000087TA0
UV1 M2@ VGA SA000098VA0
ZZZ S4G@ 4G SAMSUNG 2133 X7667538L01
ZZZ M4G@ 4G MICRON 2133 X7667538L02
ZZZ M4G2@ 4G MICRON 2400 X7667538L06
ZZZ S4G2@ 4G Samsung 2400 X7672938L04
ZZZ H4G@ 4G Hynix 2400 X7672938L05

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Notes List

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M1-70 VRAM STRAP

	Vendor UV3, UV4, UV5, UV6	ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV21	R_pd RV24
						X76@	X76@
JS2G@ X7667538L03	Samsung 4096Mbits 2GBytes SA000076P80 256MX16 K4W4G1646E-BC1A	0	0	0	0	NC	4.75K
JM2G@ X7667538L04	Micron 4096Mbits 2GBytes SA00009HF00 256Mx16 MT41J256M16LY-091G:N	1	0	0	1	8.45K	2K
JH2G@ X7667538L05	Hynix 4096Mbits 2GBytes SA00008DN00 256MX16 H5TC4G63CFR-N0C	2	0	1	0	4.53K	2K
		4	1	0	0	4.53K	4.99K
		5	1	0	1	3.24K	5.62K
		6	1	1	0	3.4K	10K

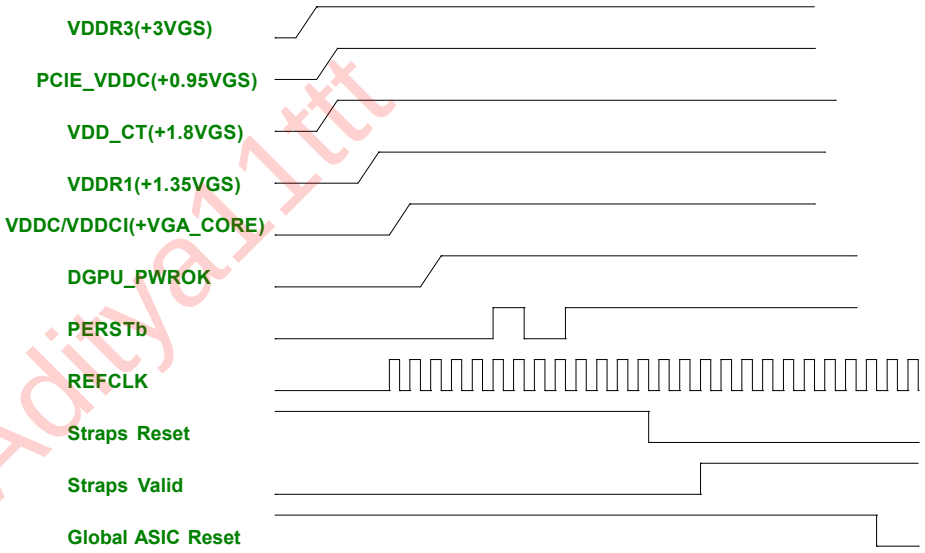
R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Power-Up/Down Sequence

"M1" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μ s.
- It is recommended that the 3.3-V rail ramp up frist.
- It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2ms from the start of VDDC ramping up.
- The power rails that are shared with other components on the system should be gated for the dGPU so that when dGPU is powered down (for example AMD PowerXpressTM idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≦ 50mV/us)
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



Security Classification	Compal Secret Data		Compal Electronics, Inc.
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Title	VGA Notes List		
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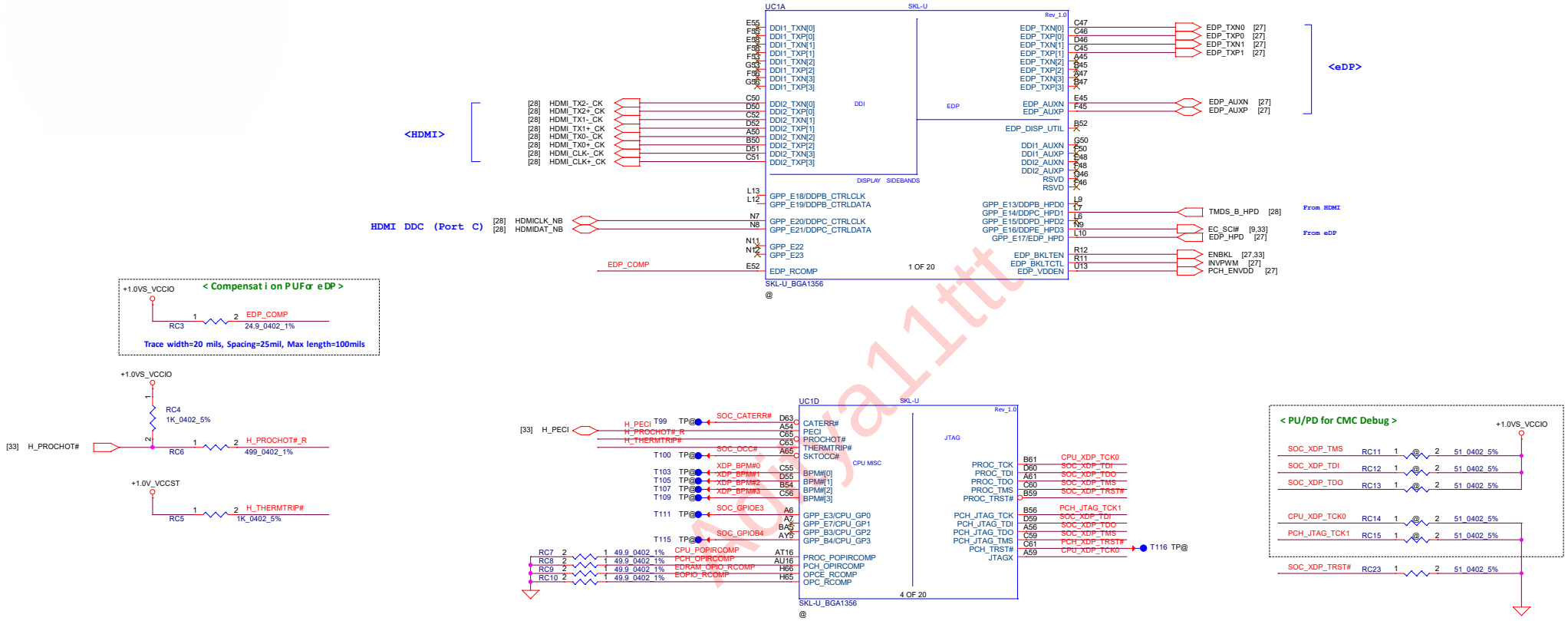

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Compal Electronics, Inc.			
Title: SKL-U(1/12)DDI,EDP,MISC,CMC			
Size: Custom	Document Number: LA-D562P		Rev: 2.0
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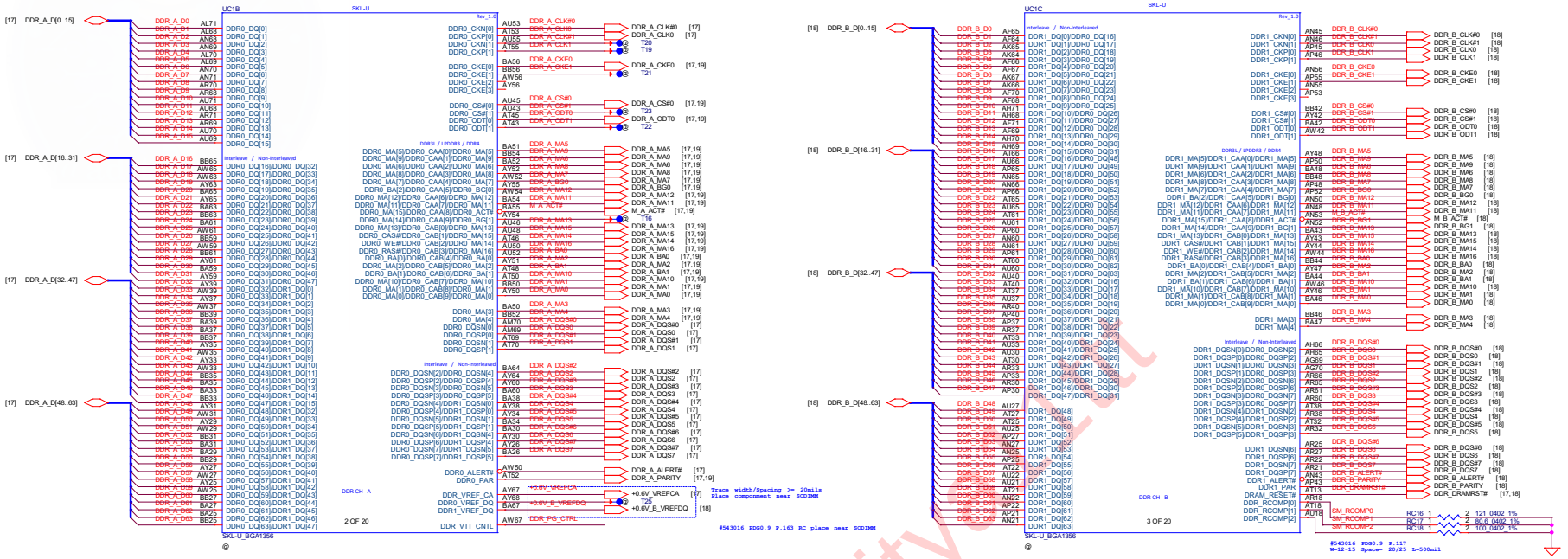
Interleaved Memory



Security Classification	Compal Secret Data		
Issued Date	2015/01/29	Deciphered Date	2016/01/29

Compal Electronics, Inc.			
Title: SKL-U(2/12)DDR3L			
Size: Custom	Document Number: LA-D562P		Rev: 2.0
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SMBALERT# (Internal Pull Down):

0 = Disable Intel ME TLS function ==> Default

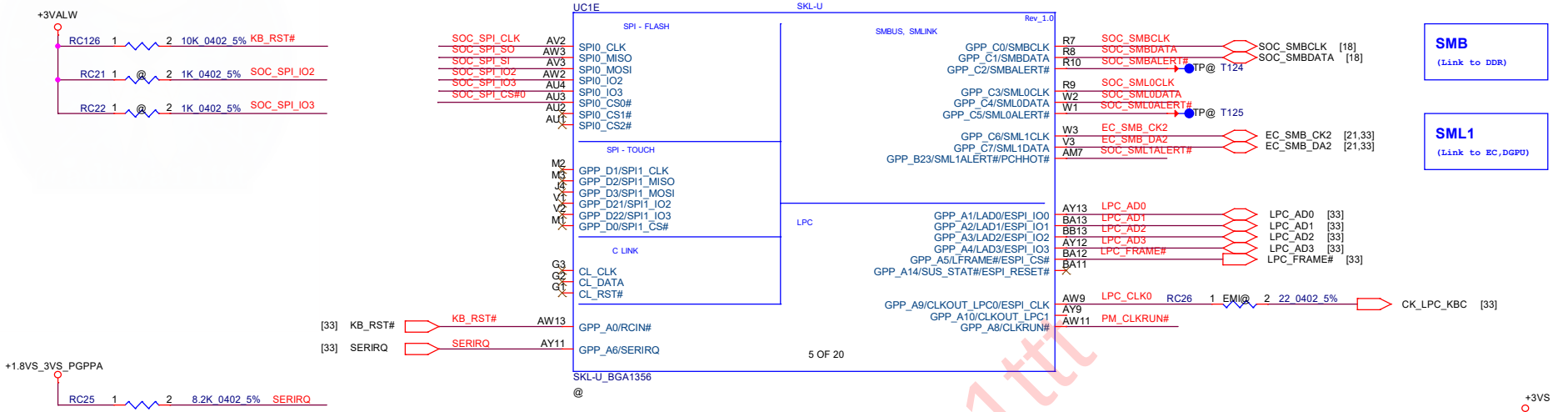
1 = Enable Intel ME TLS function

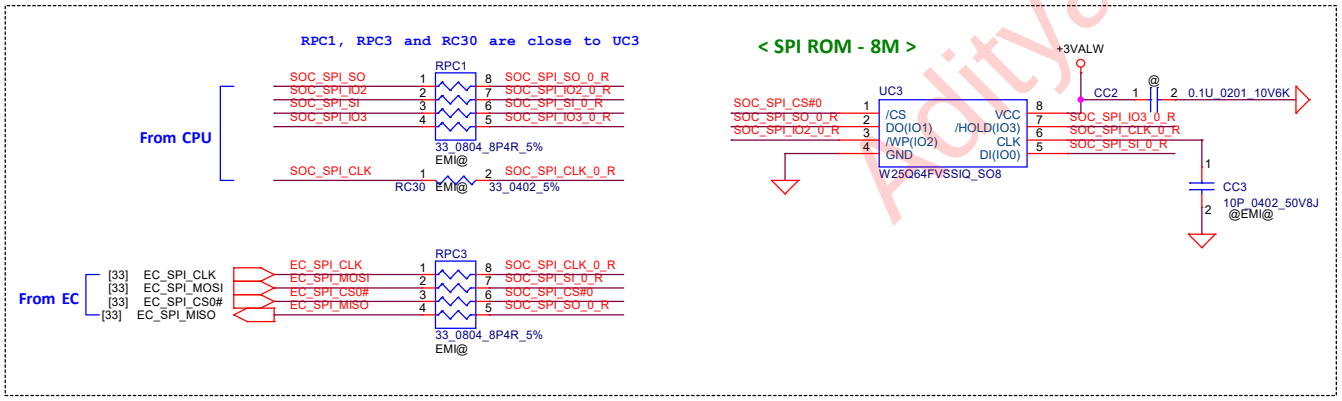
SML0ALERT# (Internal Pull Down):

eSPI or LPC

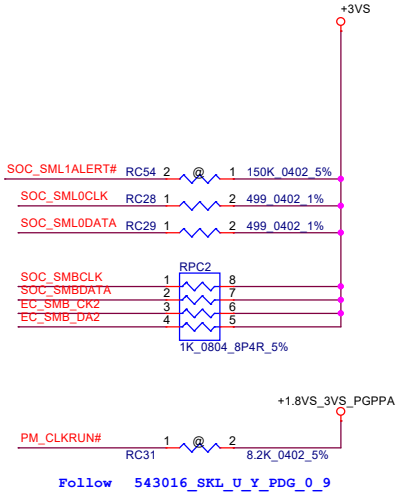
0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC





< SPI ROM - 8M >



Follow 543016_SKL_U_Y_PDG_0_9

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,SMB,LPC,ESPI

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< HD AUDIO >

RPC4

[35] HDA_BITCLK_AUDIO
[35] HDA_SYNC_AUDIO
[35] HDA_SDOUT_AUDIO
[35] HDA_RST_AUDIO#

1 → 8 HDA_BIT_CLK
2 → 7 HDA_SYNC
3 → 6 ME_EN
4 → 5 HDA_RST#

33_0804_8P4R_5%
EMI@

< To Enable ME Override > [33] ME_EN
[35] HDA_SDIN0

UC1G SKL-U Rev_1.0

AUDIO

HDA_SYNC BA22 HDA_SYNC/I2S0_SFRM
HDA_BIT_CLK AY22 HDA_BLK/I2S0_SCLK
ME_EN BB22 HDA_SDO/I2S0_TXD
BA21 HDA_SDI0/I2S0_RXD
AY21 HDA_SDI1/I2S1_RXD
HDA_RST# AW22 HDA_RST#/I2S1_SCLK
J5 GPP_D23/I2S_MCLK
AY20 I2S1_SFRM
AW20 I2S1_TXD

AK7 GPP_F1/I2S2_SFRM
AK8 GPP_F0/I2S2_SCLK
AK9 GPP_F2/I2S2_TXD
AK10 GPP_F3/I2S2_RXD

H5 GPP_D19/DMIC_CLK0
D7 GPP_D20/DMIC_DATA0

D8 GPP_D17/DMIC_CLK1
C8 GPP_D18/DMIC_DATA1

[35] HDA_SPKR HDA_SPKR AW5 GPP_B14/SPKR

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SKL-U_BGA1356
@

SDIO / SDXC

GPP_G0/SD_CMD AB11
GPP_G1/SD_DATA0 AB13
GPP_G2/SD_DATA1 AB12
GPP_G3/SD_DATA2 W12
GPP_G4/SD_DATA3 W11
GPP_G5/SD_CD# W10
GPP_G6/SD_CLK W8
GPP_G7/SD_WP W7

GPP_A17/SD_PWR_EN#/ISH_GP7 BA9
GPP_A16/SD_1P8_SEL BB9

SD_RCOMP AB7 RC109 2 @ 1 200_0402_1%

GPP_F23 AF13

+3VS

1 @ 2 HDA_SPKR
RC33 2.2K_0402_5%

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.

UC1I SKL-U Rev_1.0

CSI-2

A36 CSI2_DN0
B36 CSI2_DP0
C38 CSI2_DN1
D38 CSI2_DP1
C36 CSI2_DN2
D36 CSI2_DP2
A38 CSI2_DN3
B38 CSI2_DP3

C31 CSI2_DN4
D31 CSI2_DP4
C33 CSI2_DN5
D33 CSI2_DP5
A31 CSI2_DN6
B31 CSI2_DP6
A33 CSI2_DN7
B33 CSI2_DP7

A29 CSI2_DN8
B29 CSI2_DP8
C28 CSI2_DN9
D28 CSI2_DP9
A27 CSI2_DN10
B27 CSI2_DP10
C27 CSI2_DN11
D27 CSI2_DP11

CSI2_CLKN0 C37
CSI2_CLKP0 D37
CSI2_CLKN1 C32
CSI2_CLKP1 D32
CSI2_CLKN2 C29
CSI2_CLKP2 D29
CSI2_CLKN3 B26
CSI2_CLKP3 A26

CSI2_COMP E13 RC117 2 @ 1 100_0402_1%
GPP_D4/FLASHTRIG B7

EMMC

GPP_F13/EMMC_DATA0 AP2
GPP_F14/EMMC_DATA1 AP1
GPP_F15/EMMC_DATA2 AP3
GPP_F16/EMMC_DATA3 AN3
GPP_F17/EMMC_DATA4 AN1
GPP_F18/EMMC_DATA5 AN2
GPP_F19/EMMC_DATA6 AM4
GPP_F20/EMMC_DATA7 AM1

GPP_F21/EMMC_RCLK AM2
GPP_F22/EMMC_CLK AM3
GPP_F12/EMMC_CMD AP4

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EMMC_RCOMP AT1 RC116 2 @ 1 200_0402_1%

SKL-U_BGA1356
@

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

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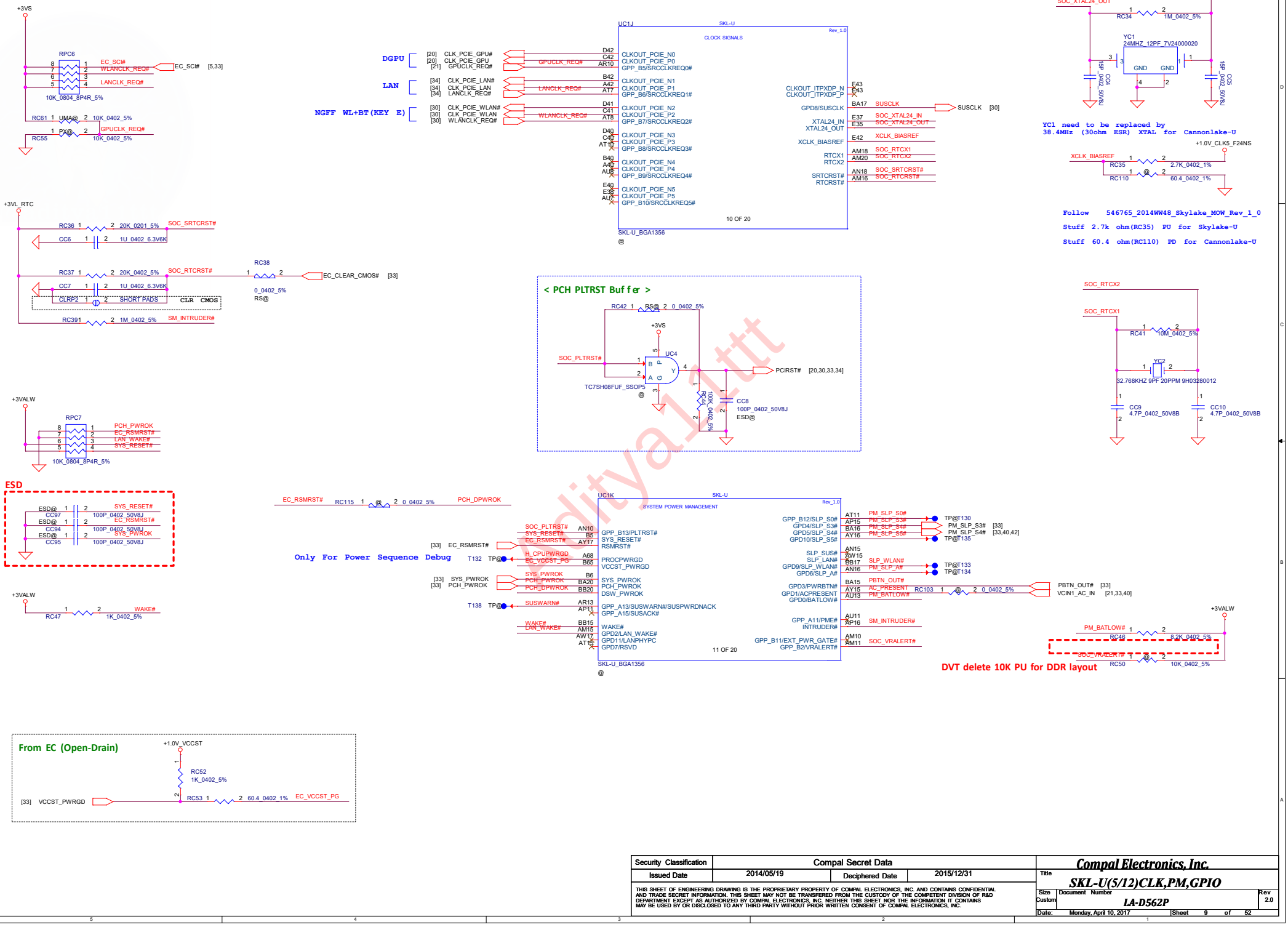

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	SKL-U(5/12)CLK,PM,GPIO		
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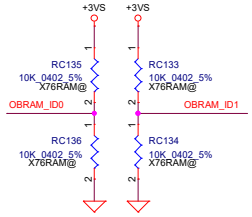
SKL

RAM vender	OBRAM_ID0	OBRAM_ID1
Samsung K4A8G165WB-BCPB	0	0
Micron MT40A512M16HA-083E:A	0	1
Micron MT40A512M16JY-083E:B		
	1	0
	1	1

KBL

RAM vender	OBRAM_ID0	OBRAM_ID1
Samsung K4A8G165WB-BCRC	0	0
Micron MT40A512M16JY-083E:B	0	1
Hynix H5AN8G6NAFR-UHC	1	0
	1	1



GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

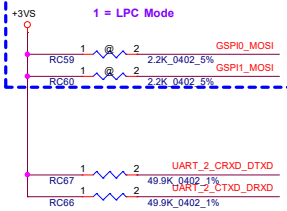
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

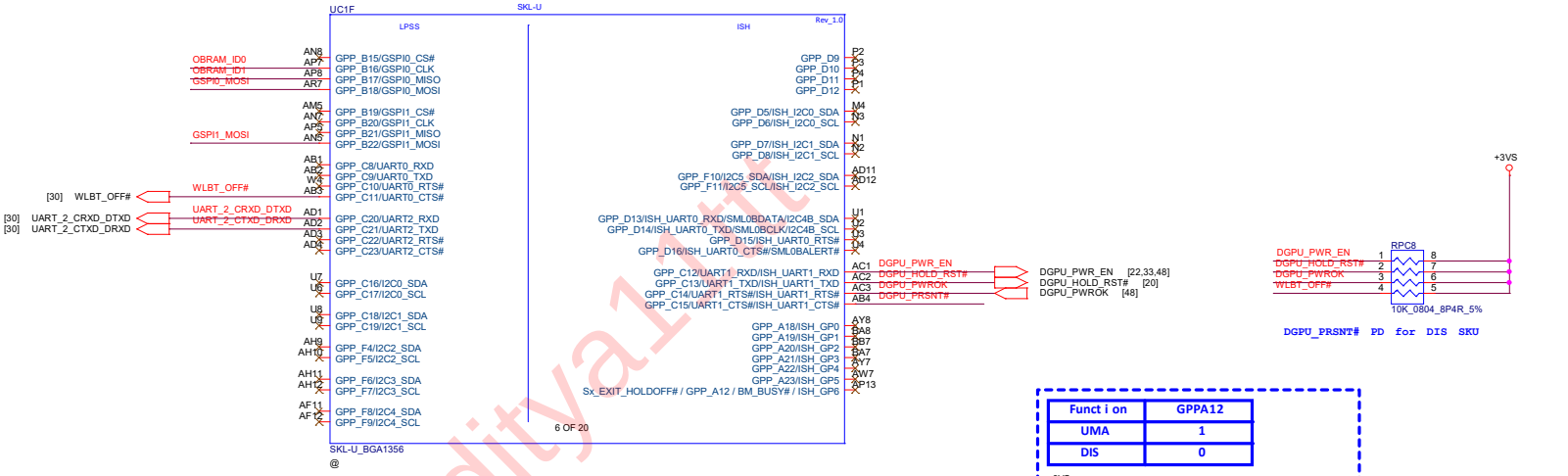
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode ==> Default

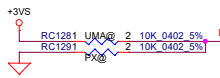
1 = LPC Mode





DGPU_PRSNT# PD for DIS SKU

Funct i on	GPPA12
UMA	1
DIS	0



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Compal Electronics, Inc.

Title: SKL-U(6/12)GPIO,I2C,GSPI

Size	Document Number	Rev
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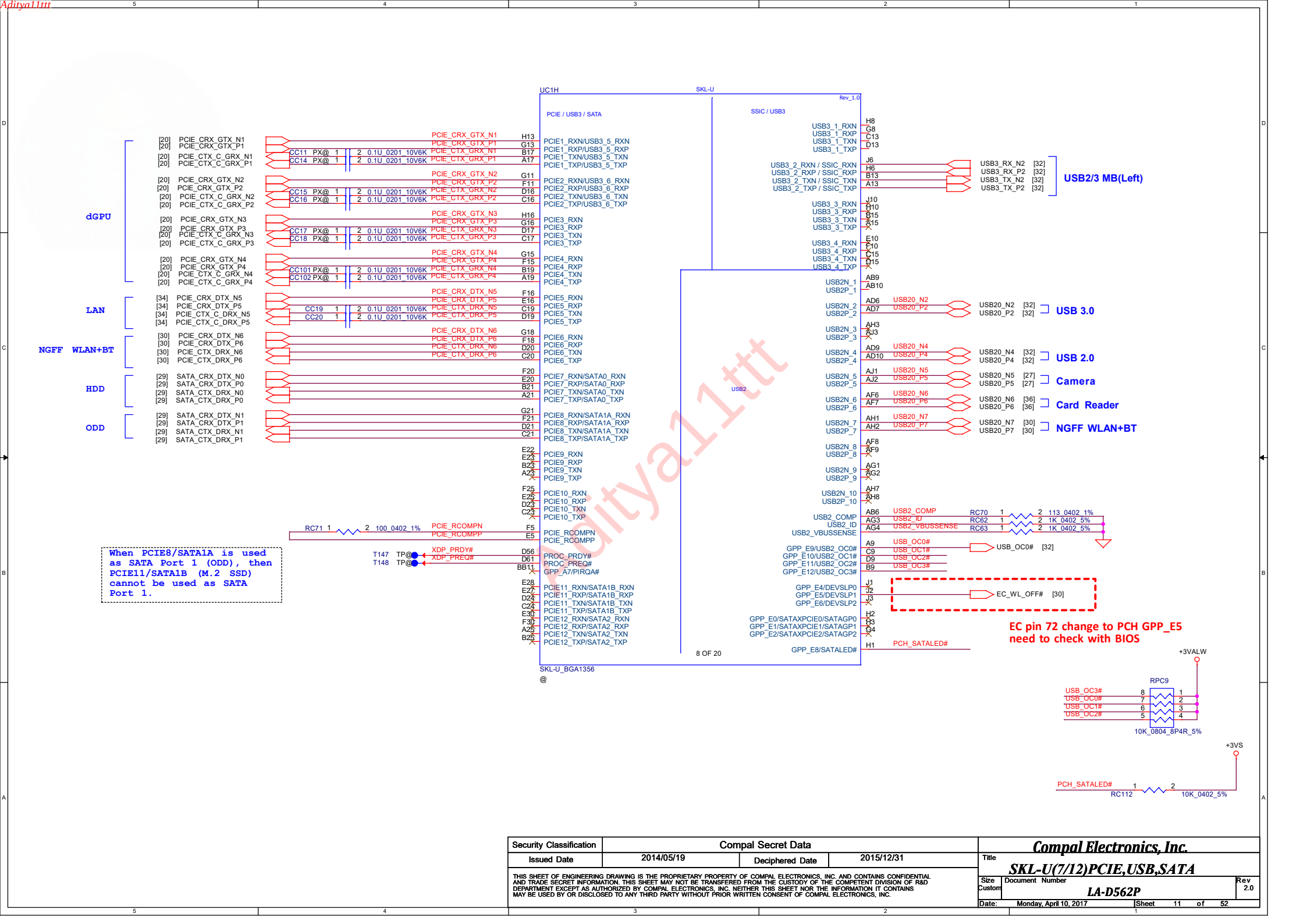

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Compal Electronics, Inc.			
Title	SKL-U(7/12)PCIE,USB,SATA		
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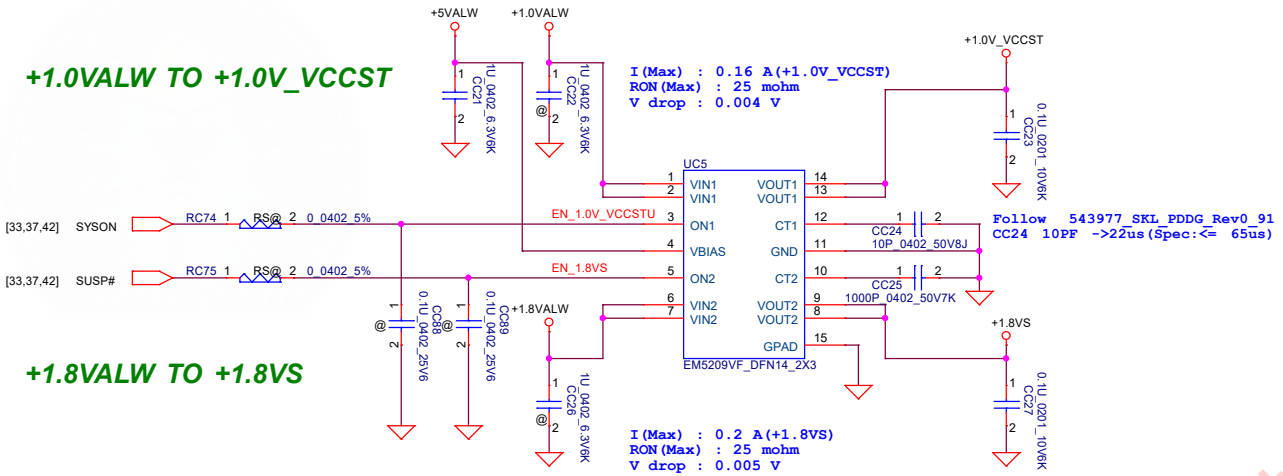
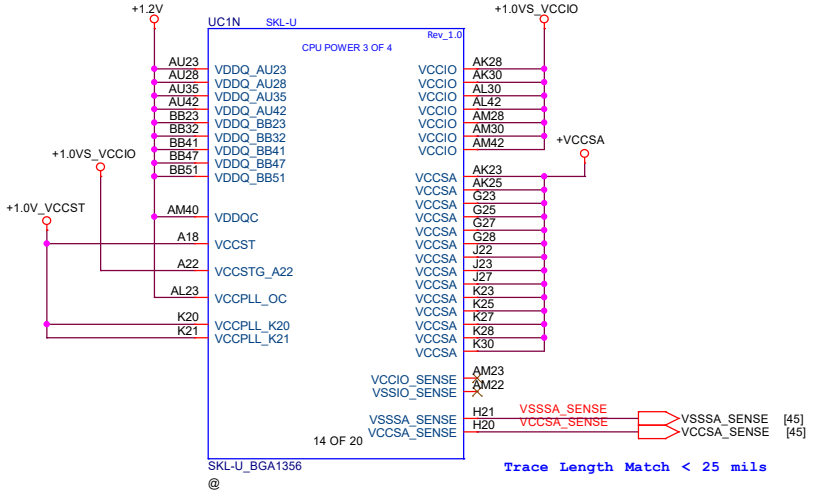
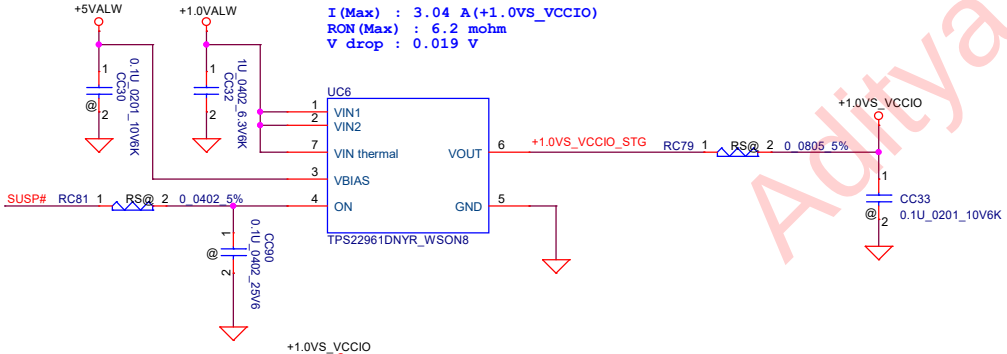
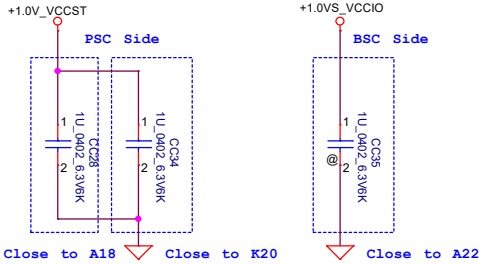
+1.0VALW TO +1.0V_VCCST

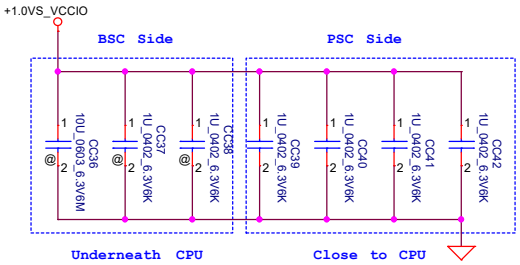


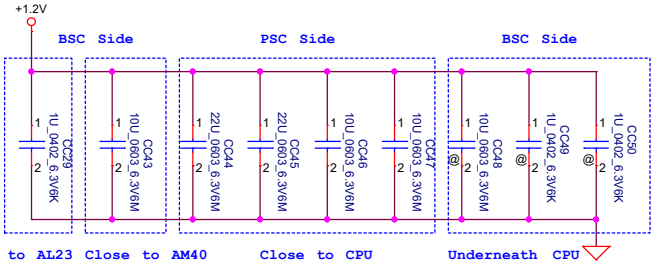


+1.0VALW TO +1.0VS_VCCIO









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Compal Electronics, Inc.			
Title: SKL-U(8/12)Power			
Size: Custom	Document Number: LA-D562P		Rev: 2.0
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Follow 543016_SKL_U_Y_PDG_1_0

+1.0VALW
LC1
MURATA BLM15EG221SN1D
SM01000HC00
R_0402 RF@
+1.0V_APLL
CC52 0.1U_0201_10V K X5R RF@

Follow 543016_SKL_U_Y_PDG_1_0

+1.0V_AMPHYPLL
LC2 RS@ 0_0603_5%
22U_0603_6.3V6M CC58 @
1U_0402_6.3V6K CC59

Follow 543016_SKL_U_Y_PDG_1_0

+1.0V_CLK5_F24NS
RC85 RS@ 0_0603_5%
22U_0603_6.3V6M CC83

Follow 543016_SKL_U_Y_PDG_1_0

+1.0V_CLK4_F100OC
RC87 RS@ 0_0603_5%
22U_0603_6.3V6M CC70

Follow 543016_SKL_U_Y_PDG_1_0

+1.0V_CLK6_24TBT
RC91 RS@ 0_0603_5%
1U_0402_6.3V6K CC84
22U_0603_6.3V6M CC85

+1.0VALW
RC83 RS@ 0_0805_5%
Imax : 2.57A
+1.0V_PRIM_CORE
1U_0402_6.3V6K CC54 @

RC84 RS@ 0_0805_5%
Imax : 3.5A
+1.0V_MPHYGT
22U_0603_6.3V6M CC80 @
1U_0402_6.3V6K CC81

+3VALW
RC86 RF@
MURATA BLM15EG221SN1D
SM01000HC00
R_0402
+1.8V_HDA
0.1U_0201_10V K X5R CC86 RF@

HD Audio : 3.3V or 1.5V
I2S : 1.8V or 3.3V

+1.8VALW
RC88 @ 0_0402_5%
+3V_1.8V_PGPPA
+3VALW
LPC 3.3V
RC89 RS@ 0_0402_5%

+1.8VS
RC92 @ 0_0402_5%
+1.8VS_3VS_PGPPA
+3VS
LPC 3.3V
RC93 RS@ 0_0402_5%

+3VALW
CC87 2.2U_0402_6.3V6K
Close to AJ21

+1.0VALW
CC88 2.2U_0402_6.3V6K
Close to AF20

CC89 2.2U_0402_6.3V6K
Close to N18

Follow 543016_SKL_U_Y_PDG_1_0

+1.0VALW
22U_0603_6.3V6M CC71 CC72
+3VALW
22U_0603_6.3V6M CC73 CC74
+1.8VALW
22U_0603_6.3V6M CC75 CC76

+1.0VALW
CC51 2 1U_0402_6.3V6K @
+1.0V_PRIM_CORE
CC55 2 1U_0402_6.3V6K
CC56 2 1U_0402_6.3V6K
Close to K17
+1.0V_MPHYGT
+1.0V_AMPHYPLL
+1.0V_APLL
+3VALW
+1.8V_HDA
+3VALW

UC1O SKL-U
CPU POWER 4 OF 4
Rev_1.0

AB19	VCCPRIM_1P0	VCCPGPPA	AK15
AB20	VCCPRIM_1P0	VCCPGPPB	AG15
P18	VCCPRIM_1P0	VCCPGPPC	Y16
AF18	VCCPRIM_CORE	VCCPGPPD	Y15
AF19	VCCPRIM_CORE	VCCPGPPE	T16
V20	VCCPRIM_CORE	VCCPGPPF	AF16
V21	VCCPRIM_CORE	VCCPGPPG	AD15
	VCCPRIM_CORE		
DCPDSW	AL1	VCCPRIM_3P3	V19
	DCPDSW_1P0		
	K17	VCCPRIM_1P0	T1
L1	VCCMPHYAON_1P0		
	VCCMPHYAON_1P0	VCCATS_1P8	AA1
	N15		AK17
N16	VCCMPHYGT_1P0_N15	VCCRTCPRIM_3P3	
N17	VCCMPHYGT_1P0_N16		AK19
P15	VCCMPHYGT_1P0_N17	VCCRTC_AK19	BB14
P16	VCCMPHYGT_1P0_P15	VCCRTC_BB14	
	VCCMPHYGT_1P0_P16		BB10
K15		DCPRTC	
L15	VCCAMPHYPLL_1P0		A14
	VCCAMPHYPLL_1P0	VCCCLK1	
V15			K19
	VCCAPLL_1P0	VCCCLK2	
AB17			L21
Y18	VCCPRIM_1P0_AB17	VCCCLK3	
	VCCPRIM_1P0_Y18		N20
AD17		VCCCLK4	
AD18	VCCDSW_3P3_AD17		L19
AJ17	VCCDSW_3P3_AD18	VCCCLK5	
	VCCDSW_3P3_AJ17		A10
AJ19		VCCCLK6	
AJ16	VCCHDA		AN11
	VCCSPI	GPP_B0/CORE_VID0	AN13
AF20		GPP_B1/CORE_VID1	
AF21	VCCSRAM_1P0		
T19	VCCSRAM_1P0		
T20	VCCSRAM_1P0		
	VCCSRAM_1P0		
AJ21			
	VCCPRIM_3P3_AJ21		
AK20			
	VCCPRIM_1P0_AK20		
N18			
	VCCAPLLEBB_1P0		

15 OF 20
SKL-U_BGA1356

+3V_1.8V_PGPPA
VCCPGPPF support 1.8V only
+1.0VALW
CC57 2 1U_0402_6.3V6K
+3VL_RTC
DCPRTC CC62 2 0.1U_0201_10V6K
+1.0V_CLK6_24TBT
+1.0V_APLL
+1.0V_CLK4_F100OC
+1.0V_CLK5_F24NS
+1.0V_CLK6_24TBT

Delete CC77 , CC78 for DDR layout modify

+3VALW
CC90 1U_0402_6.3V6K
Close to AG15

CC91 1U_0402_6.3V6K
Close to Y16

Close to T16

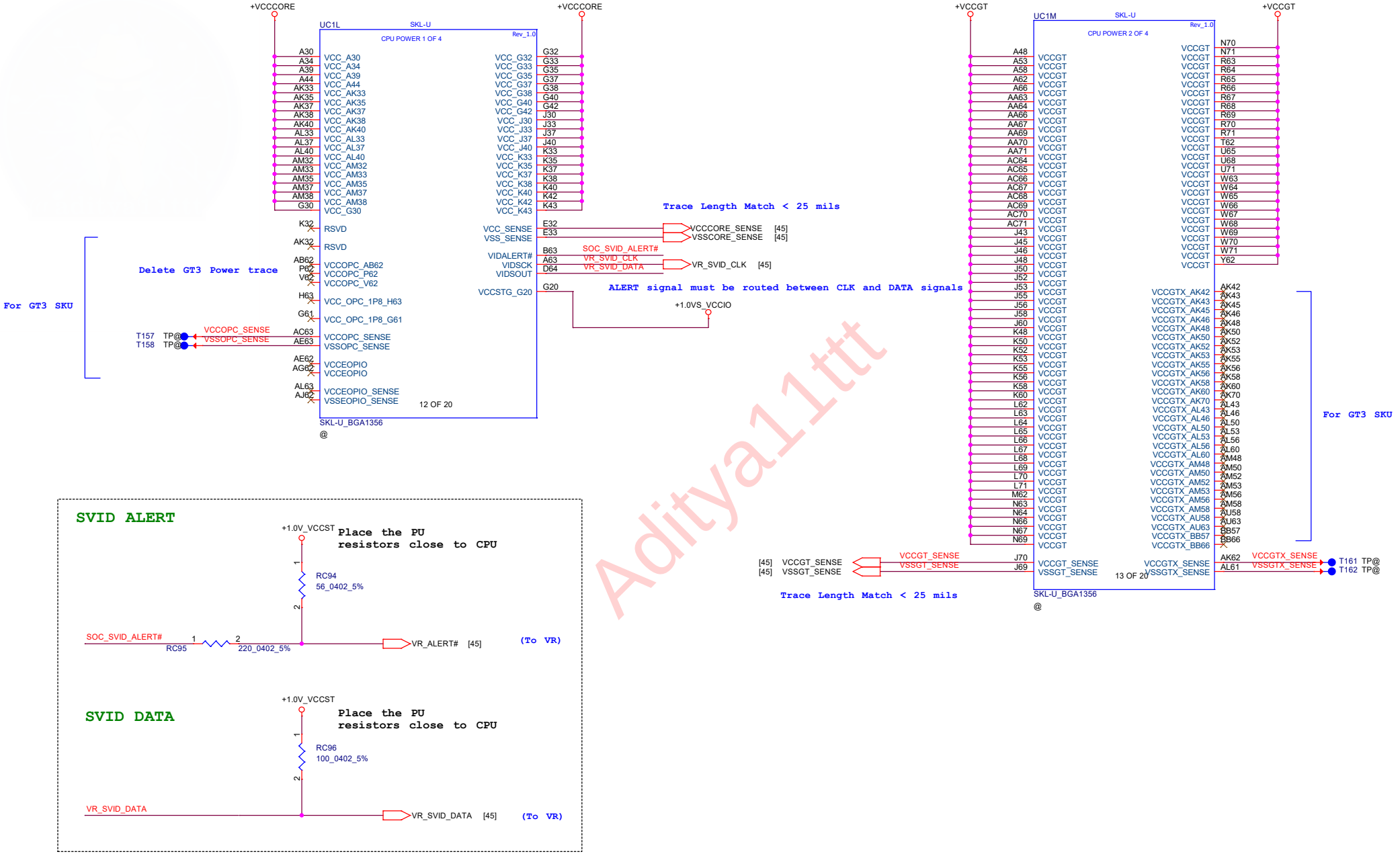
CC81 1U_0402_6.3V6K
Close to AK17

CC79 0.1U_0201_10V6K

RTC Battery
+3VL_RTC
+RTCBATT
W=20mils
RC90 1 RS@ 2 0_0402_5%
CC82 1U_0402_6.3V6K
Safty suggestion remove Eside, Keep PWside

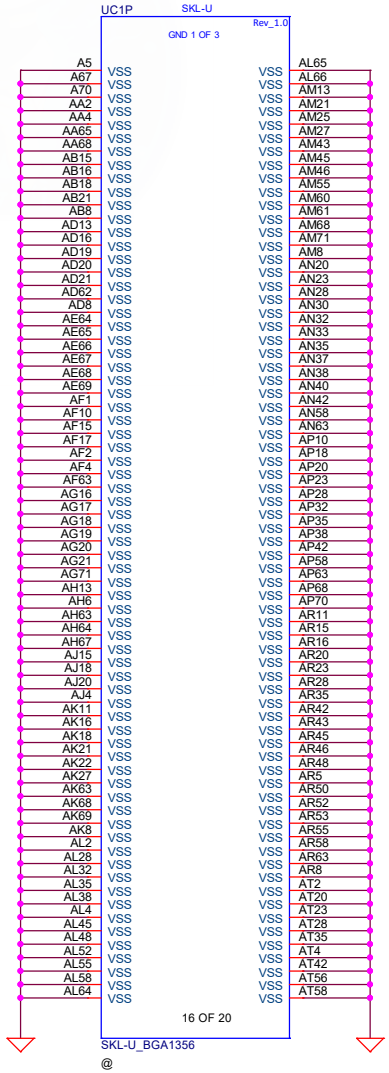
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

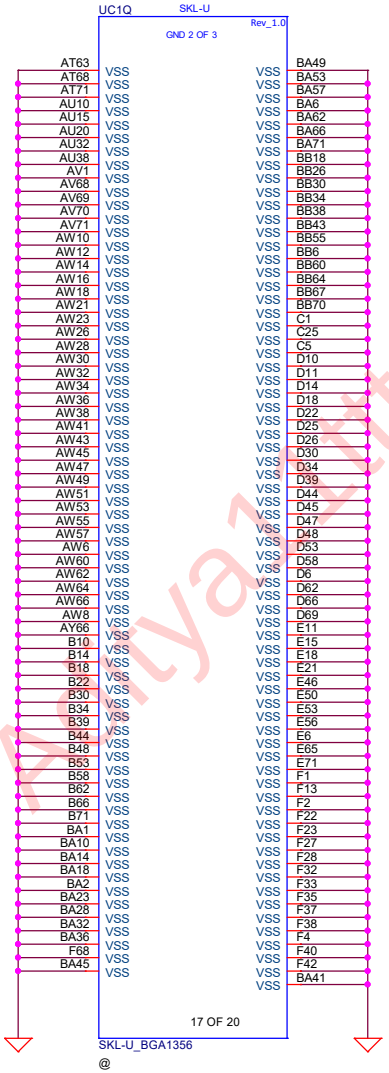
Compal Electronics, Inc.			
Title	SKL-U(9/12)Power		
Size	Document Number		Rev
Custom	LA-D562P		2.0
Date:	Monday, April 10, 2017	Sheet	13 of 52

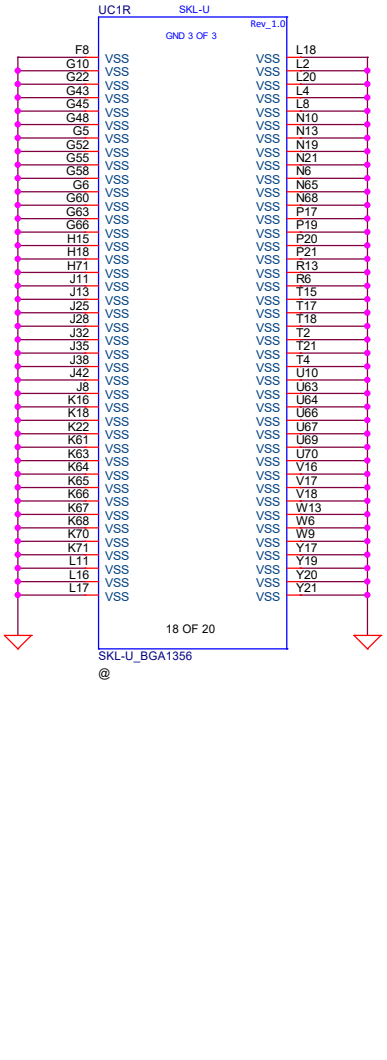


Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	SKL-U(10/12)Power,SVID		
Size	Document Number		Rev
Custom	LA-D562P		2.0
Date:	Monday, April 10, 2017	Sheet	14 of 52







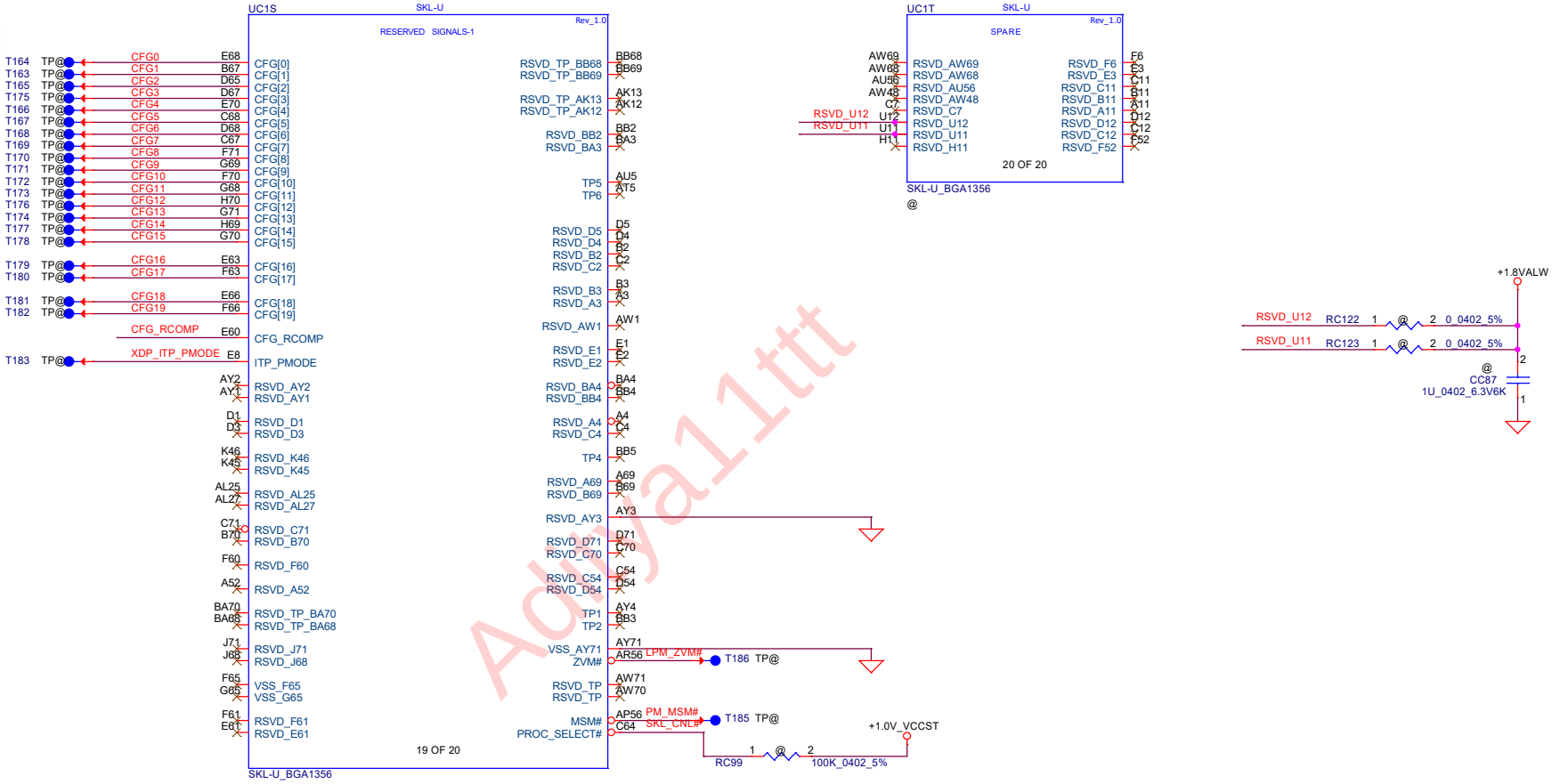
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **SKL-U(11/12)GND**

Size	Document Number	Rev
Custom	LA-D562P	2.0

Date: Monday, April 10, 2017 Sheet 15 of 52



Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1.0

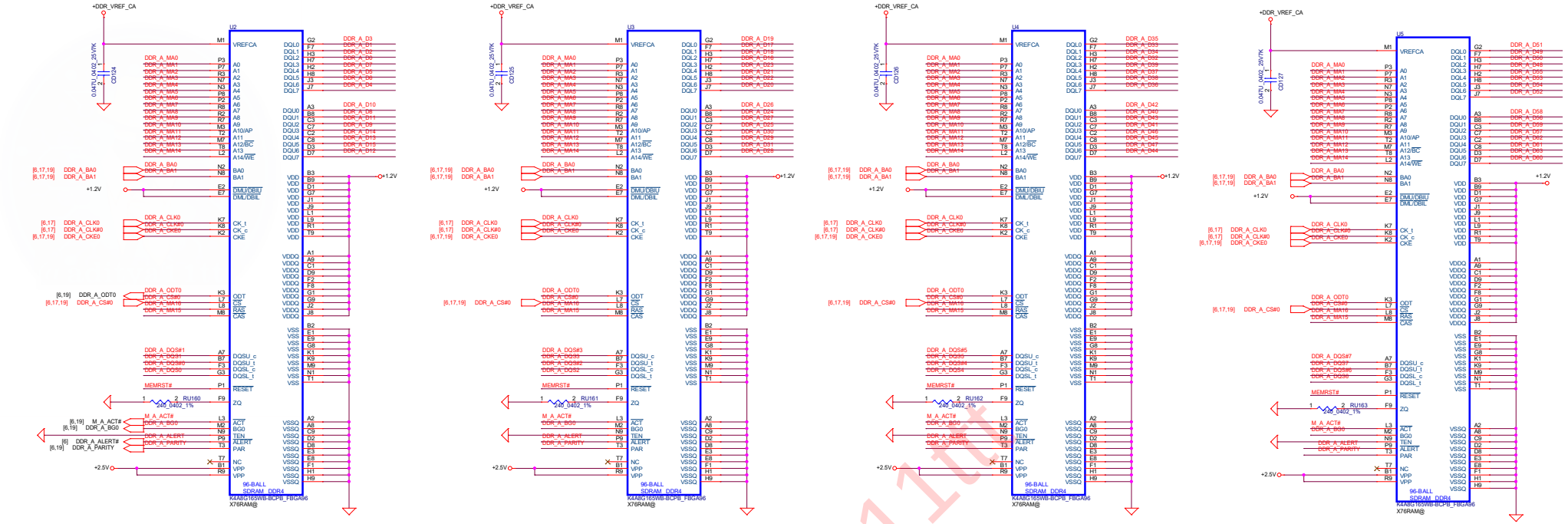
Stuff 100k(RC99) for Cannonlake.

Un-stuff 100k(RC99) for Skylake

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

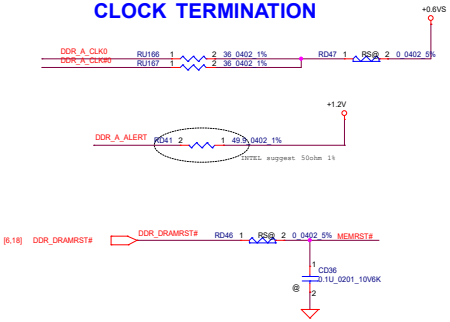
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

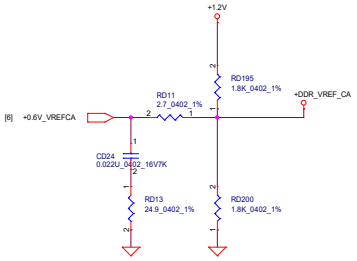
Compal Electronics, Inc.			
Title: SKL-U(12/12)CFG,RSVD			
Size: Custom	Document Number: LA-D562P		Rev: 2.0
Date: Monday, April 10, 2017	Sheet 16 of 52		



[6,19] DDR_A_MA[0..16]
[6] DDR_A_DQS#[0..7]
[6] DDR_A_DQS[0..7]
[6] DDR_A_D[0..63]

CLOCK TERMINATION





Data mapping

U2	DQ	U3	DQ	U4	DQ	U5	DQ
DQL0	D3	DQL0	D19	DQL0	D35	DQL0	D51
DQL1	D1	DQL1	D17	DQL1	D33	DQL1	D49
DQL2	D2	DQL2	D18	DQL2	D34	DQL2	D50
DQL3	D0	DQL3	D16	DQL3	D32	DQL3	D48
DQL4	D7	DQL4	D23	DQL4	D39	DQL4	D55
DQL5	D5	DQL5	D21	DQL5	D37	DQL5	D53
DQL6	D6	DQL6	D22	DQL6	D38	DQL6	D54
DQL7	D4	DQL7	D20	DQL7	D36	DQL7	D52
DQU0	D10	DQU0	D26	DQU0	D42	DQU0	D58
DQU1	D8	DQU1	D24	DQU1	D40	DQU1	D56
DQU2	D11	DQU2	D27	DQU2	D43	DQU2	D59
DQU3	D9	DQU3	D25	DQU3	D41	DQU3	D57
DQU4	D14	DQU4	D30	DQU4	D46	DQU4	D62
DQU5	D13	DQU5	D29	DQU5	D45	DQU5	D61
DQU6	D15	DQU6	D31	DQU6	D47	DQU6	D63
DQU7	D12	DQU7	D28	DQU7	D44	DQU7	D60

Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Title	DDR4 ON BOARD CHIPS		
Size	Document Number		Rev
Custom	LA-D562P		2.0
Date:	Monday, April 10, 2017	Sheet	17 of 52

Reverse Type

2-3A to 1 DIMMs/channel

[6] DDR_B_DQS#[0..7]
[6] DDR_B_D[0..63]
[6] DDR_B_DQS[0..7]

[6] DDR_B_MA[0..16]
[6] DDR_B_BA0 — DDR_B_BA0
[6] DDR_B_BA1 — DDR_B_BA1
[6] DDR_B_BG0 — DDR_B_BG0
[6] DDR_B_BG1 — DDR_B_BG1

[6] DDR_B_CLK0 — DDR_B_CLK0
[6] DDR_B_CLK#0 — DDR_B_CLK#0
[6] DDR_B_CLK1 — DDR_B_CLK1
[6] DDR_B_CLK#1 — DDR_B_CLK#1

[6] DDR_B_CKE0 — DDR_B_CKE0
[6] DDR_B_CKE1 — DDR_B_CKE1
[6] DDR_B_CS#0 — DDR_B_CS#0
[6] DDR_B_CS#1 — DDR_B_CS#1

[7] SOC_SMBDATA — SOC_SMBDATA
[7] SOC_SMBCLK — SOC_SMBCLK

[6] DDR_B_ODT0 — DDR_B_ODT0
[6] DDR_B_ODT1 — DDR_B_ODT1

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

+1.2V

CD01 CD02 CD03 CD04 CD05 CD06 CD07 CD08 CD09
1U_0402_6.3V6K

4 as near side of the DIMM close to VDD pins

CD10 CD11 CD12 CD13 CD14 CD15 CD16 CD17 CD18 CD19 CD20
10U_0603_6.3V6M

Place these caps on the VTT plane close to DIMM

+0.6VS

CD30 CD31 CD32 CD33 CD34 CD35 CD36 CD37
1U_0402_6.3V6K

+3VS

C2142 2.2U_0402_6.3V6M — +3VS_DIMM — CD28 0.1U_0201_10V6K

close to DIMM

+2.5V

C2140 10U_0603_6.3V6M — CD29 1U_0402_6.3V6K

JDIMM1

DDR_B_D14	VSS	VSS	DDR_B_D11
DDR_B_D15	VSS	VSS	DDR_B_D10
DDR_B_DQS#1	DQ1	DQ0	
DDR_B_DQS1	VSS	VSS	
	DQS0_C	DM0*/DBI0*	
DDR_B_D13	DQS0_T	VSS	DDR_B_D8
DDR_B_D12	VSS	DQ6	DDR_B_D9
DDR_B_D1	DQ7	VSS	DDR_B_D4
DDR_B_D5	VSS	DQ2	DDR_B_D0
	DQ3	VSS	
	VSS	DQ12	DDR_B_DQS#0
	DQ13	VSS	DDR_B_DQS0
DDR_B_D3	VSS	DQ8	DDR_B_D6
DDR_B_D2	DQ15	VSS	DDR_B_D7
DDR_B_D21	VSS	DQ14	DDR_B_D20
DDR_B_D17	DQ10	VSS	DDR_B_D16
DDR_B_DQS#2	DQ21	DQ20	
DDR_B_DQS2	VSS	VSS	
DDR_B_D23	DQ17	DQ16	
DDR_B_D22	VSS	VSS	DDR_B_D19
DDR_B_D29	DQS2_C	DM2*/DBI2*	DDR_B_D18
DDR_B_D25	DQS2_T	VSS	DDR_B_D28
	VSS	DQ22	DDR_B_D24
DDR_B_D30	DQ23	VSS	DDR_B_DQS#3
DDR_B_D26	VSS	DQ18	DDR_B_DQS3
	DQ19	VSS	DDR_B_D31
	VSS	DQ28	DDR_B_D27
	DQ29	VSS	
	VSS	DQ24	
	DQ25	VSS	
	VSS	DQS3_C	DDR_B_DQS#3
	DM3*/DBI3*	DQS3_T	DDR_B_DQS3
	VSS	VSS	DDR_B_D31
	DQ30	DQ31	DDR_B_D27
	VSS	VSS	
	DQ26	DQ27	
	VSS	VSS	
	CB5_NC	CB4_NC	
	VSS	VSS	
	CB1_NC	CB0_NC	
	VSS	VSS	
	DQS8_C	DM8*/DBI8*	
	DQS8_T	VSS	
	VSS	CB6_NC	
	CB2_NC	VSS	
	VSS	CB7_NC	
	CB3_NC	VSS	
DDR_B_CKE0	VSS	RESET*	DDR_B_CKE1
	CKE0	CKE1	
	VDD1	VDD2	
	BG1	ACT*	M_B_ACT# [6]
	BG0	ALERT*	DDR_B_ALERT# [6]
	VDD3	VDD4	DDR_B_MA11
	A12	A11	DDR_B_MA7
	A9	A7	
	VDD5	VDD6	DDR_B_MA5
	A8	A6	DDR_B_MA4
	A6	A4	
	VDD7	VDD8	DDR_B_MA2
	A3	A2	
	A1	EVENT*	
	VDD9	VDD10	DDR_B_CLK1
	CK0_T	CK1_T	DDR_B_CLK#1
	CK0_C	CK1_C	
	VDD11	VDD12	DDR_B_MA0
[6] DDR_B_PARITY	PARITY	A0	
DDR_B_BA1	BA1	A10_AP	DDR_B_MA10
DDR_B_CS#0	VDD13	VDD14	DDR_B_BA0
DDR_B_MA14	S0*	BA0	DDR_B_MA16
DDR_B_ODT0	A14_WE*	A16_RAS*	DDR_B_MA15
DDR_B_CS#1	VDD15	VDD16	DDR_B_MA13
DDR_B_ODT1	ODT0	A15_CAS*	
	S1*	A13	
	VDD17	VDD18	
	ODT1	S2*/C0	
	VDD19	VREFCA	
	S3*/C1	SA2	
DDR_B_D37	VSS	VSS	DDR_B_D36
DDR_B_D33	DQ37	DQ36	DDR_B_D32
	VSS	VSS	
DDR_B_DQS#4	DQ33	DQ32	
DDR_B_DQS4	VSS	VSS	
	DQS4_C	DM4*/DBI4*	
DDR_B_D38	DQS4_T	VSS	DDR_B_D39
DDR_B_D34	VSS	DQ38	DDR_B_D35
DDR_B_D44	DQ39	VSS	DDR_B_D45
DDR_B_D40	VSS	DQ34	DDR_B_D41
	DQ44	VSS	
	VSS	DQ45	DDR_B_DQS#5
	DQ40	VSS	DDR_B_DQS5
	VSS	DQ41	
	DQS5_C	DQS5_T	
DDR_B_D43	DM5*/DBI5*	VSS	DDR_B_D47
DDR_B_D42	VSS	DQ46	DDR_B_D46
DDR_B_D52	DQ47	VSS	DDR_B_D53
DDR_B_D49	VSS	DQ43	DDR_B_D48
DDR_B_DQS#6	DQ42	DQ53	
DDR_B_DQS6	VSS	VSS	
	DQ48	DQ49	
	VSS	DQ52	
	DQS6_C	DM6*/DBI6*	
DDR_B_D55	DQS6_T	VSS	DDR_B_D54
DDR_B_D50	VSS	DQ54	DDR_B_D51
DDR_B_D61	DQ55	VSS	DDR_B_D60
DDR_B_D56	VSS	DQ50	DDR_B_D57
	DQ61	VSS	
	VSS	DQ57	DDR_B_DQS#7
	DQ56	VSS	DDR_B_DQS7
	VSS	DQS7_C	
DDR_B_D59	DM7*/DBI7*	DQS7_T	DDR_B_D63
DDR_B_D58	VSS	VSS	DDR_B_D62
SOC_SMBCLK	DQ62	DQ63	SOC_SMBDATA
+3VS_DIMM	VSS	DQ59	
	SCL	SDA	
	VDDSPD	SA0	
	VPP1	VTT	
	VPP2	SA1	
		GND	
		GND	

CONN@ FOX_AS0A827-HZSB-7H

RD166 240_0402_1% — RD166 240_0402_1%

DDR_DRAMRST#_R — CD34 0.1U_0201_10V6K

+1.2V — +DIMM_VREF_DQ

RD194 1K_0402_1%
20mil
[6] +0.6V_B_VREFDQ — RD10 2_0402_1%
CD21 0.022U_0402_16V7K
RD12 24.9_0402_1%
RD199 1K_0402_1%

RD43 470_0402_1%
DDR_DRAMRST#_R — RD45 1 — RS@ 2 0_0402_5% — DDR_DRAMRST# [6,17]

RD108 10K_0402_5%
RD138 0_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: **DDR4 DIMM**

Size: Custom | Document Number: **LA-D562P** | Rev: 2.0

Date: Monday, April 10, 2017 | Sheet 18 of 62

[6,17] DDR_A_MA[0..16]

+1.2V

4 as near each on board RAM device as possible

Follow MA51

CU89 330U_D2_2V_Y

SGA00009S00
330U 2V H1.9
9mohm POLY

+2.5V

2 as near each on board RAM device as possible

+0.6VS

2 as near each on board RAM device as possible

+0.6VS

RP17 DDR_A_MA9 DDR_A_MA5 DDR_A_MA0 DDR_A_MA1 36_0804_8P4R_5%

RP18 DDR_A_MA6 DDR_A_MA11 DDR_A_MA7 DDR_A_MA4 36_0804_8P4R_5%

RP19 DDR_A_MA14 DDR_A_MA15 DDR_A_BA0 DDR_A_BA1 36_0804_8P4R_5%
[6,17] DDR_A_BA0
[6,17] DDR_A_BA1

RP20 DDR_A_ODT0 DDR_A_CS#0 DDR_A_MA16 DDR_A_MA10 36_0804_8P4R_5%
[6,17] DDR_A_ODT0
[6,17] DDR_A_CS#0

RP21 DDR_A_BG0 DDR_A_MA12 M_A_ACT# DDR_A_CKE0 36_0804_8P4R_5%
[6,17] DDR_A_BG0
[6,17] M_A_ACT#
[6,17] DDR_A_CKE0

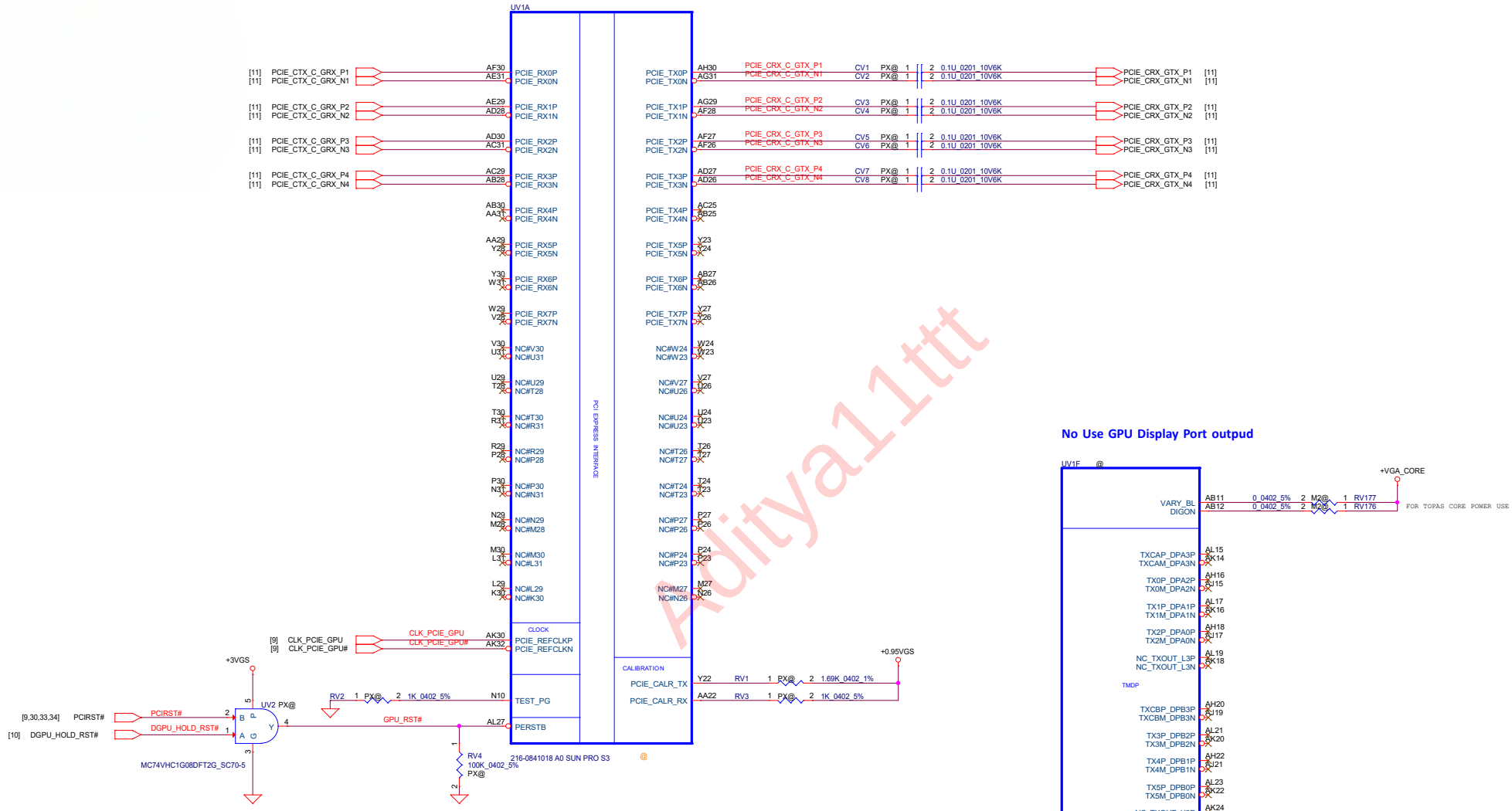
RP22 DDR_A_MA13 DDR_A_MA8 36_0804_8P4R_5%

RP24 DDR_A_MA3 DDR_A_MA2 DDR_A_PARITY 36_0804_8P4R_5%
[6,17] DDR_A_PARITY

LA-D561P Security Classification	Compal Secret Data		
Issued Date	2014/02/14	Deciphered Date	2015/02/14

Title: **DDR4 ON BOARD CHIPS**

Size: Custom	Document Number: LA-D562P	Rev: 2.0
Date: Monday, April 10, 2017	Sheet 19 of 52	



No Use GPU Display Port outpud

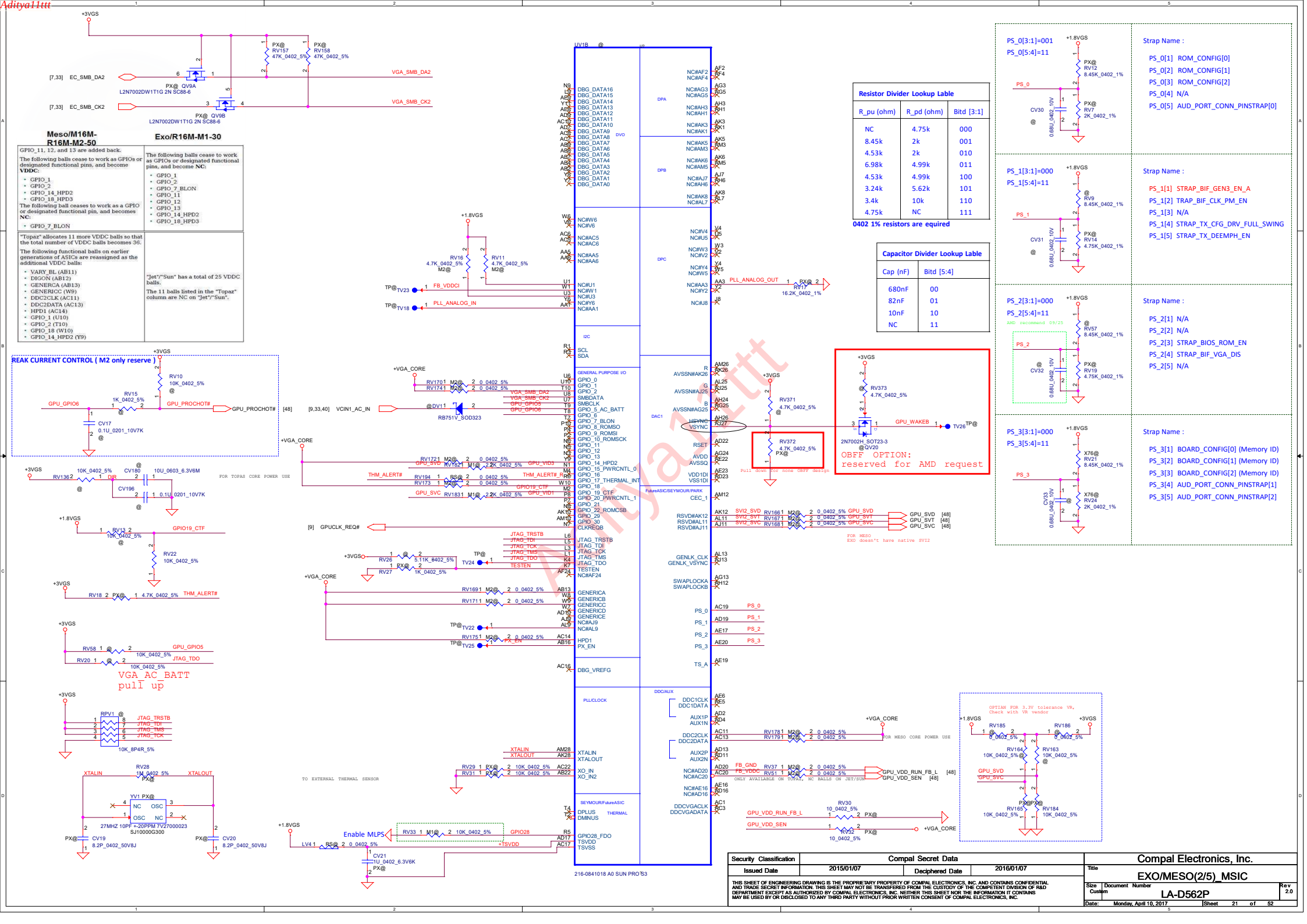
Security Classification	Compal Secret Data		
Issued Date	2015/01/07	Deciphered Date	2016/01/07

Compal Electronics, Inc.

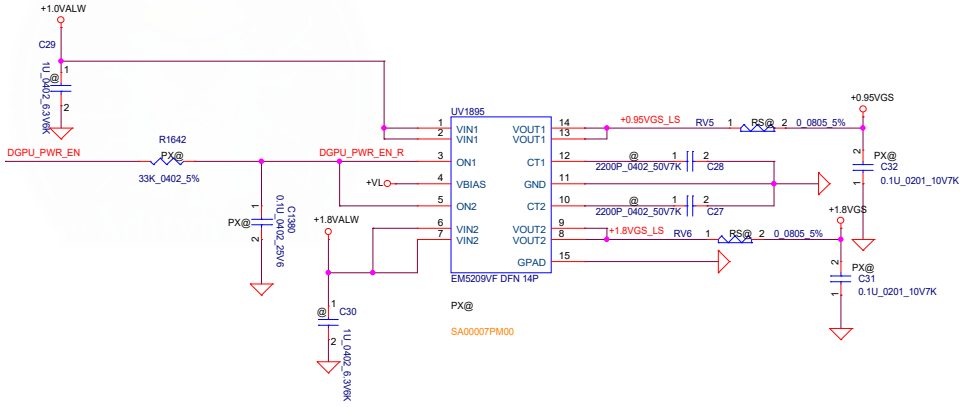
Title: R16M-M1-70(1/5)_PCIE/DP

Size	Document Number	Rev
Custom	LA-D562P	2.0

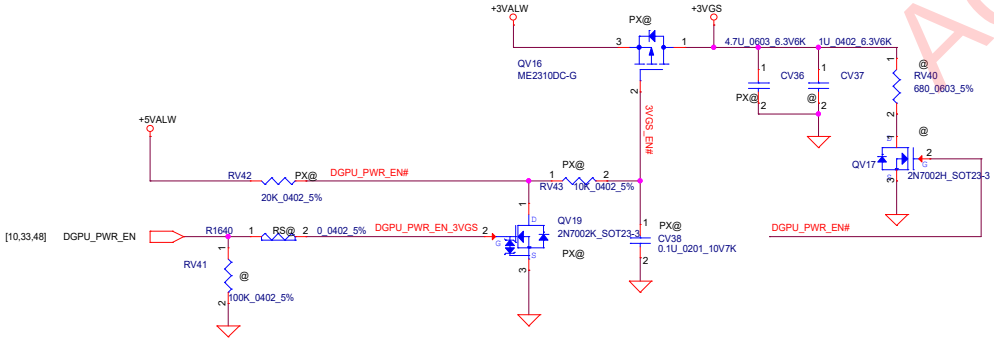
Date: Monday, April 10, 2017 Sheet 20 of 52



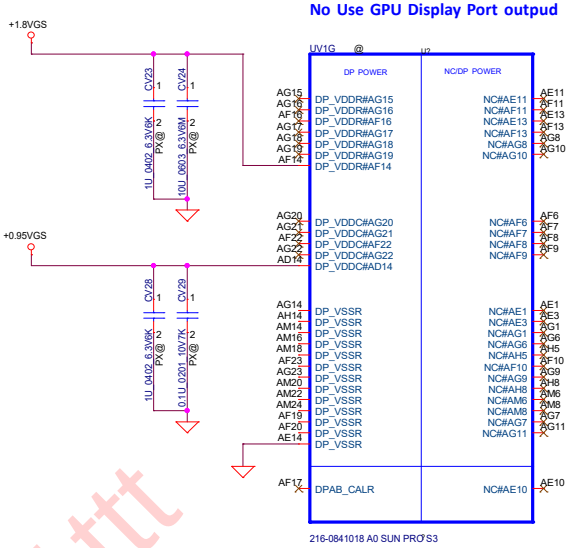
+1.8VALW TO +1.8VGS
+1.0VALW TO +1.0VGS
Load switch

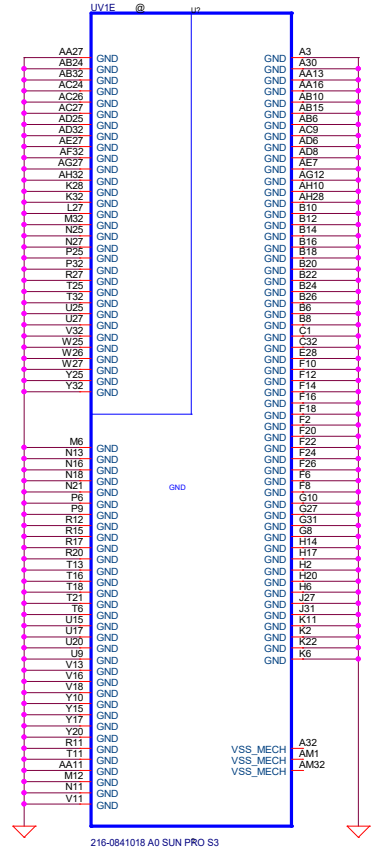


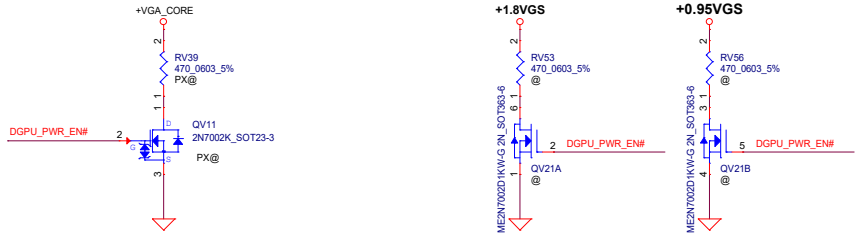
+3VS to +3VGS



No Use GPU Display Port outpud







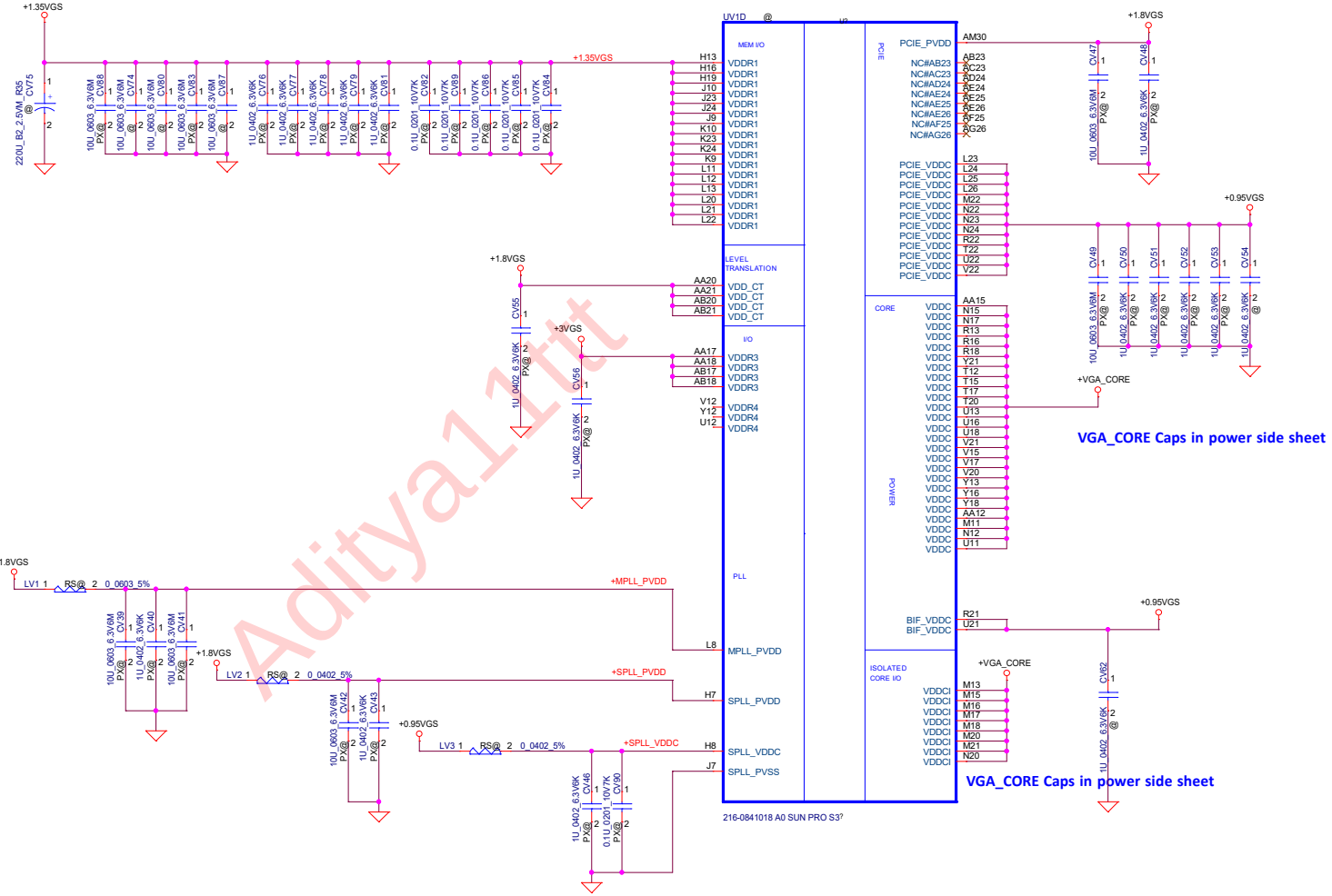
Security Classification	Compal Secret Data		
Issued Date	2015/01/07	Deciphered Date	2016/01/07

Compal Electronics, Inc.

Title: EXO/MESO(3/5)_PWR/GND

Size	Document Number	Rev
Custom	LA-D562P	2.0

Date: Monday, April 10, 2017 | Sheet 22 of 52



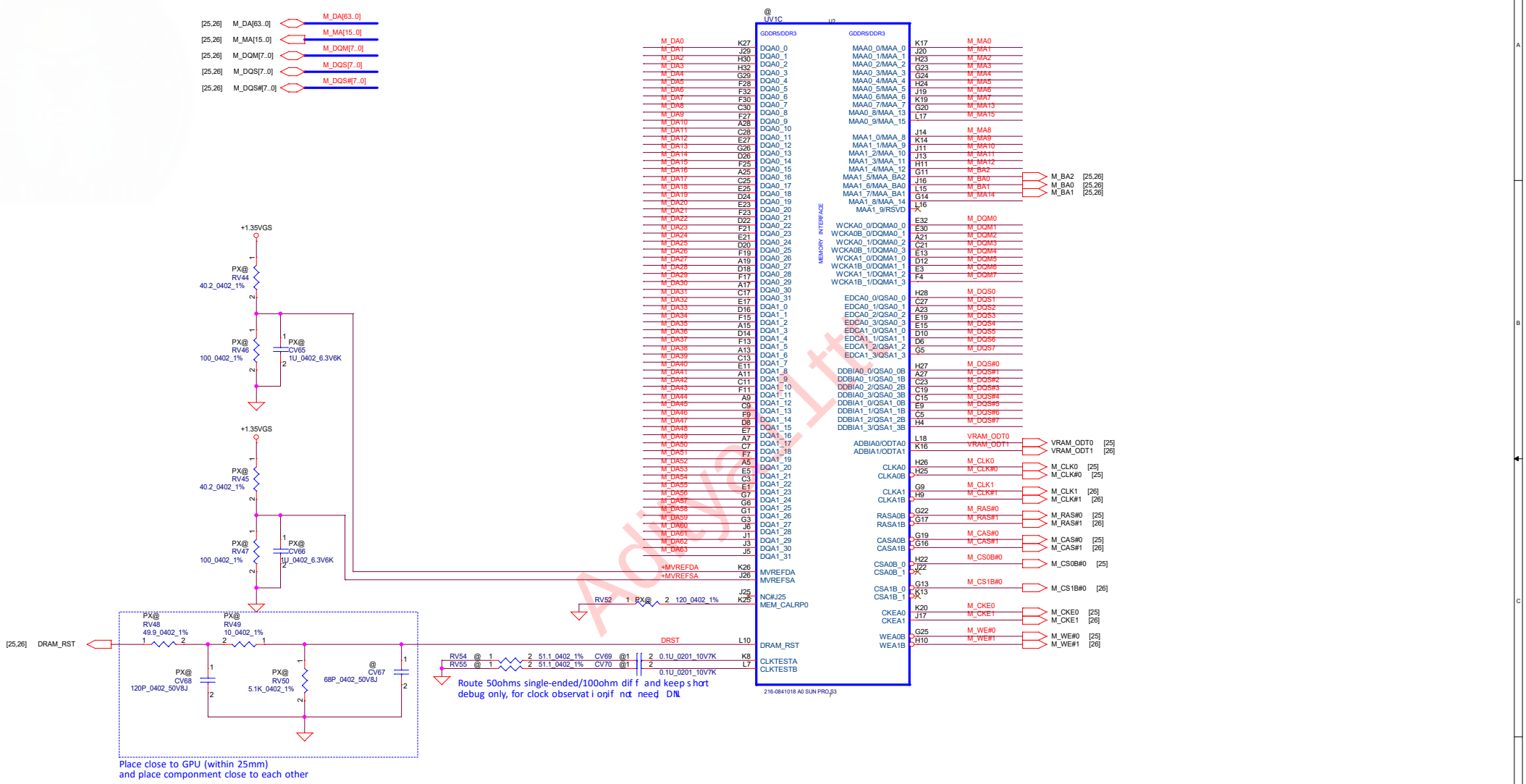
Security Classification	Compal Secret Data		
Issued Date	2015/01/07	Deciphered Date	2016/01/07

Compal Electronics, Inc.

Title: EXO/MESO(4/5)_PWR

Size	Document Number	Rev
Custom	LA-D562P	2.0

Date: Monday, April 10, 2017 | Sheet 23 of 52



Security Classification	Compal Secret Data		
Issued Date	2015/01/07	Deciphered Date	2016/01/07

Compal Electronics, Inc.

Title: EXO/MESO(5/5)_MEM

Size	Document Number	Rev
Custom	LA-D562P	2.0

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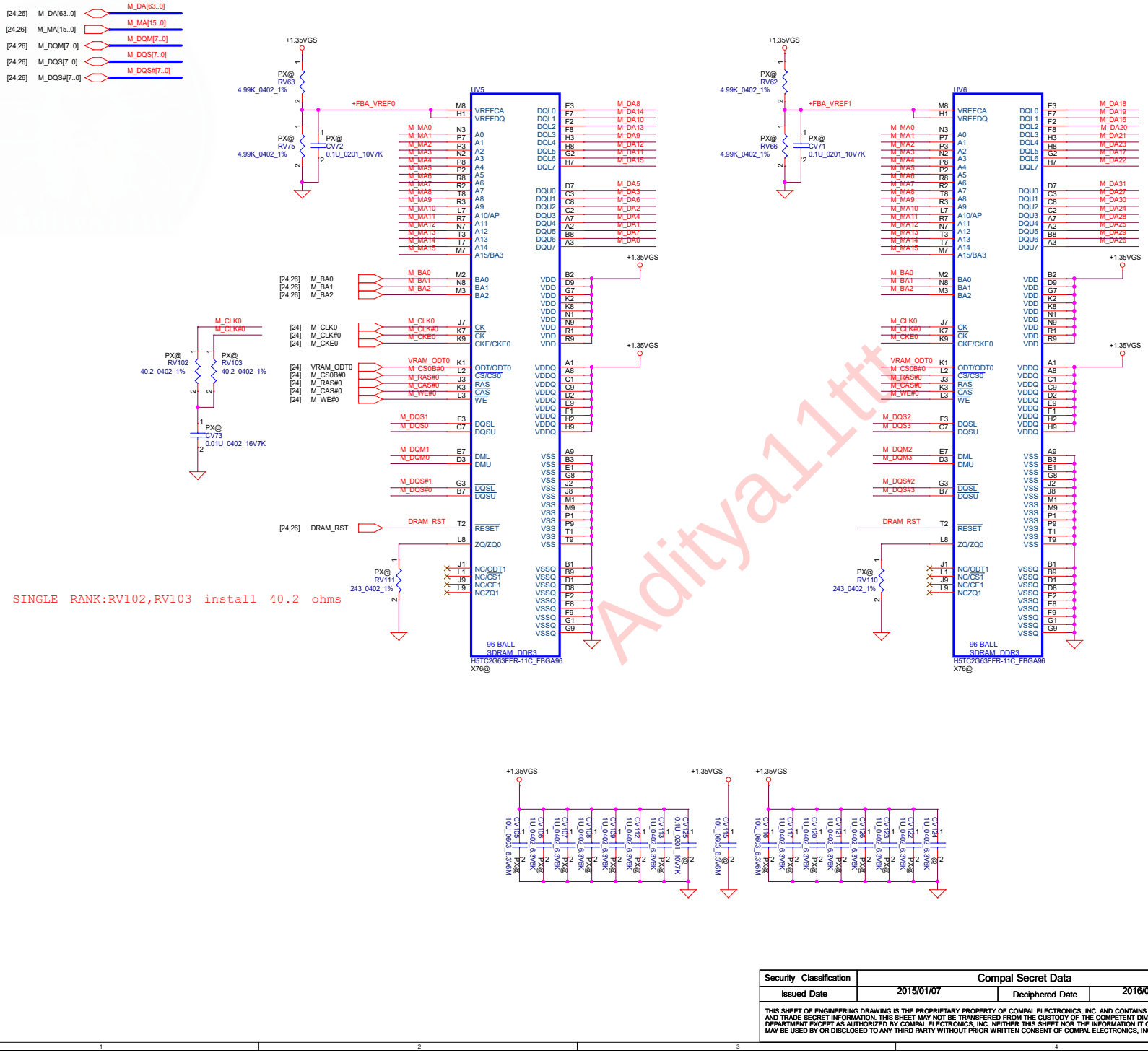
DDR3L Memory Channel Rank 0:A0



Security Classification	Compal Secret Data		
Issued Date	2015/01/07	Deciphered Date	2016/01/07

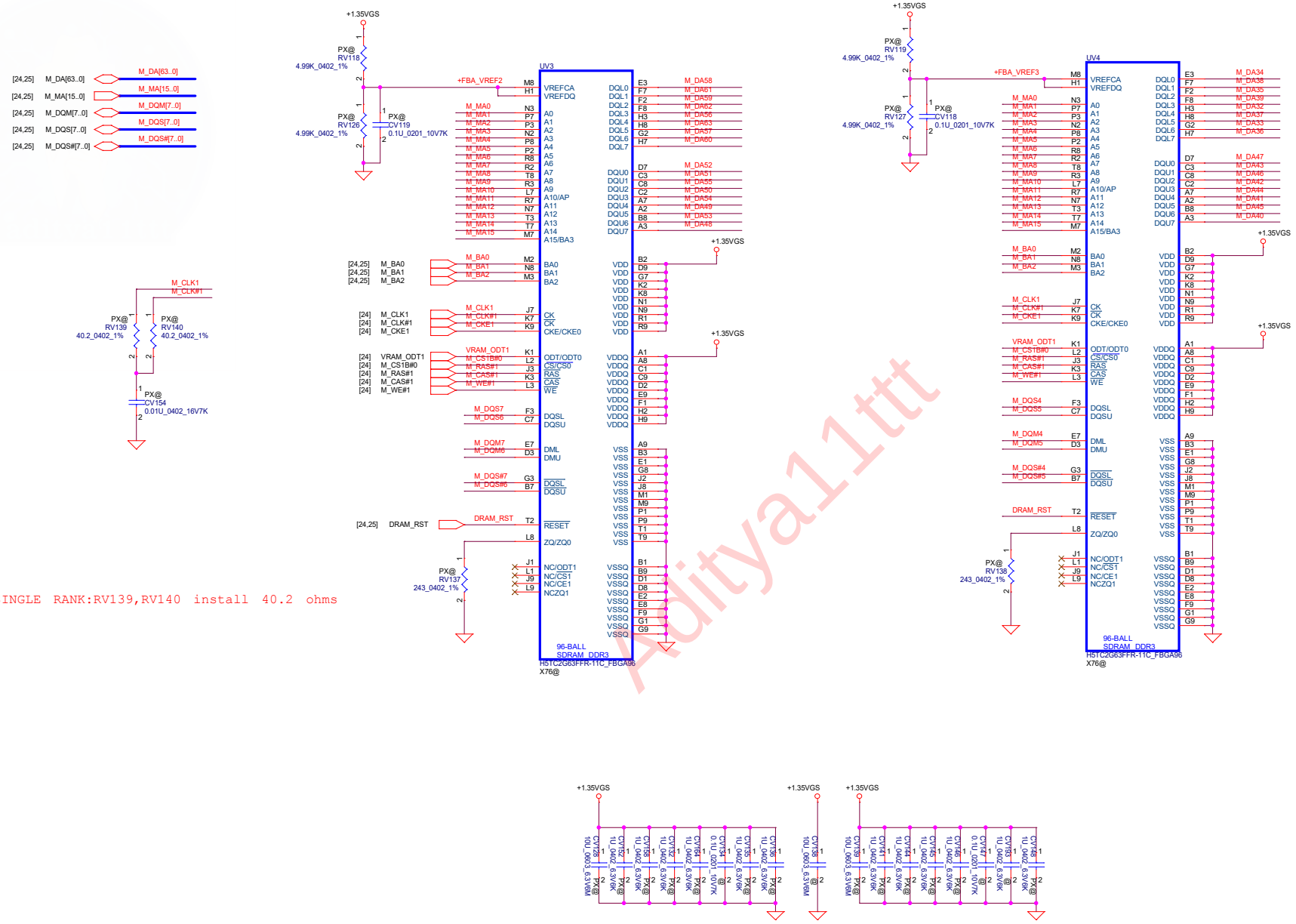
Compal Electronics, Inc.

Title: EXO/MESO_DDR3L_A1 Rank 0

Size	Document Number	Rev
Custom	LA-D562P	2.0

Date: Monday, April 10, 2017 Sheet 25 of 52

DDR3L Memory Channel Rank 0:A1



Security Classification	Compal Secret Data		
Issued Date	2015/01/07	Deciphered Date	2016/01/07

Compal Electronics, Inc.

Title: EXO/MESO_DDR3L_A2 Rank 0

Size	Document Number	Rev
Custom	LA-D562P	2.0

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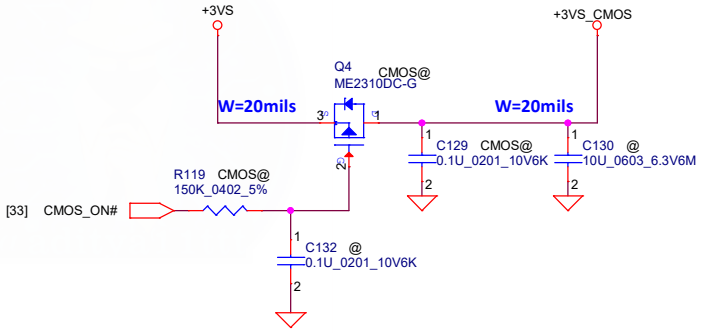
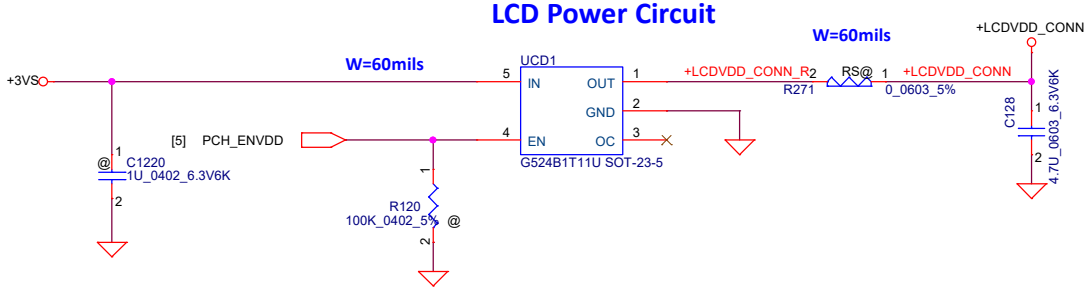
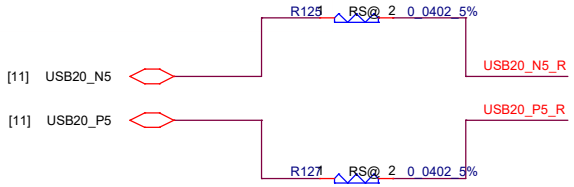
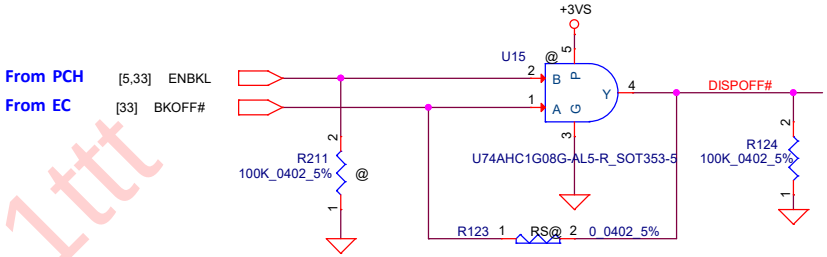
Camera



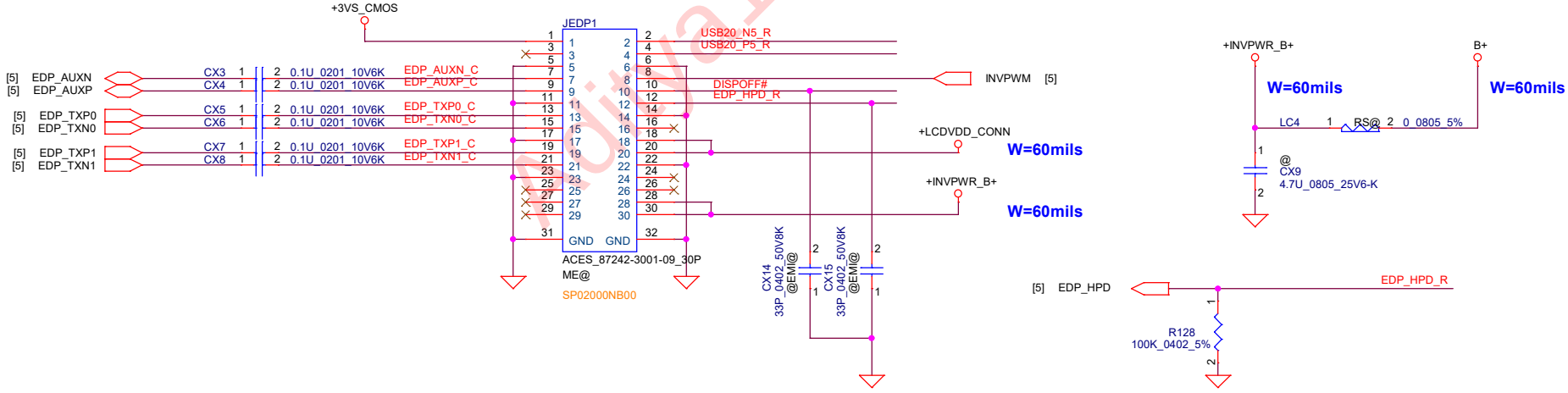
LCD Power Circuit







eDP PANEL Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

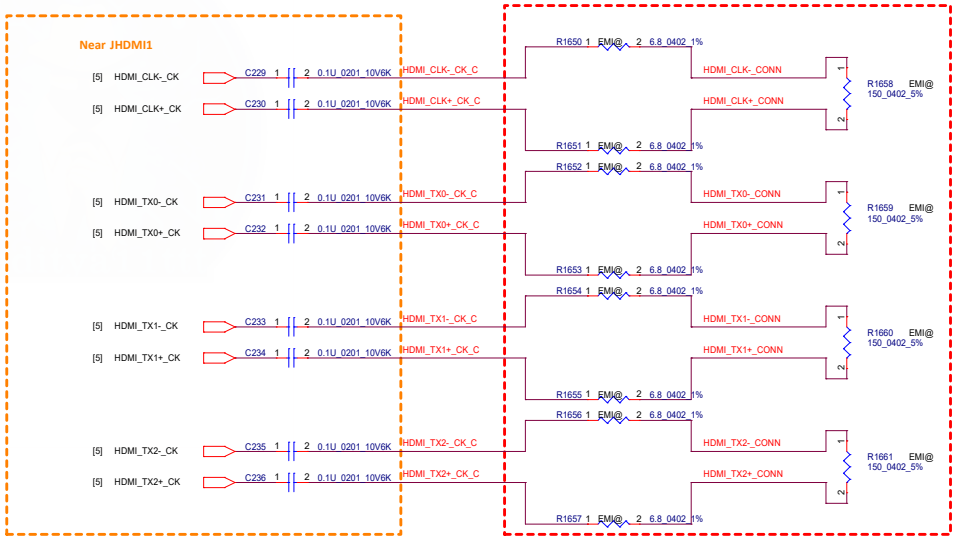
Title: **eDP/CAMERA**

Size	Document Number	Rev
B	LA-D562P	2.0

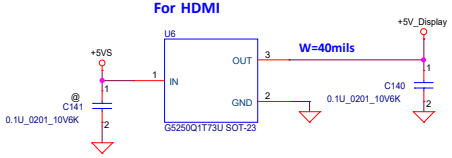
Date: Monday, April 10, 2017 Sheet 27 of 52

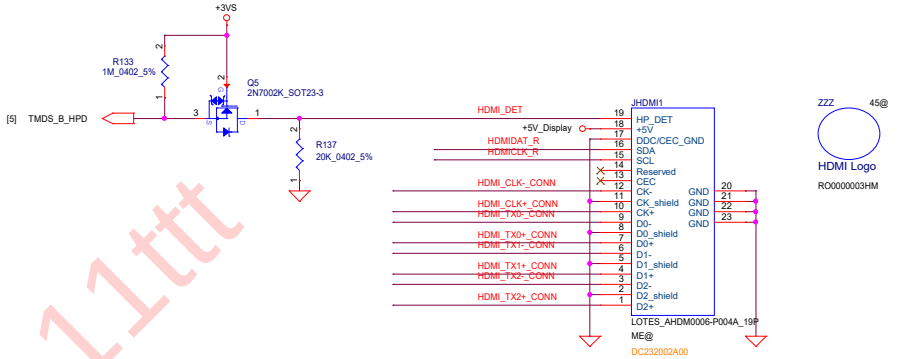
EMI

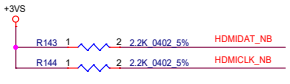
Near JHDMI1



For HDMI





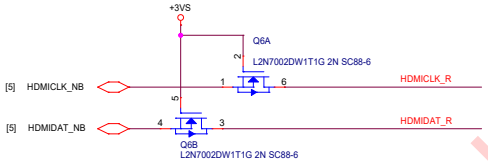


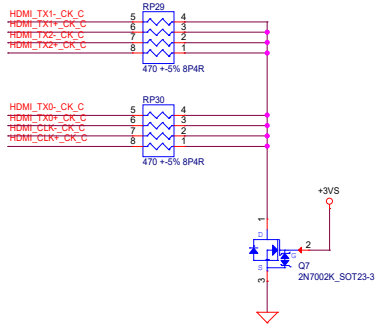
HDMIDAT_NB(Internal Pull Down):

Display Port C Detected

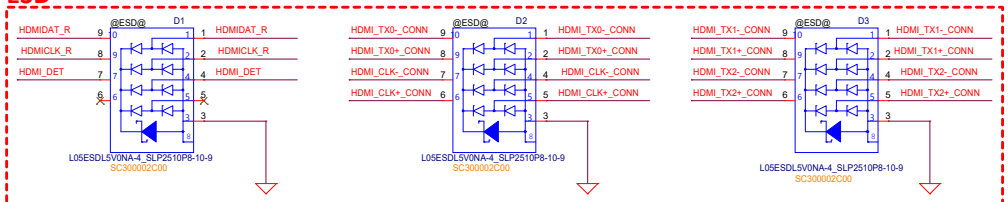
0 = Port C is not detected.

1 = Port C is detected.





ESD



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

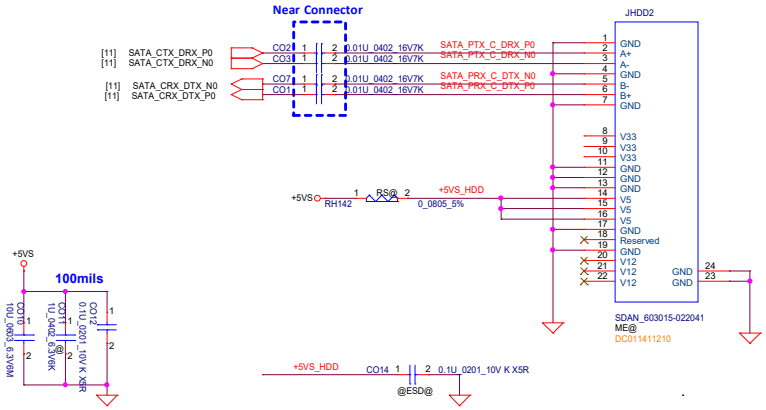
Title: **HDMI CONN**

Size	Document Number	Rev
C	LA-D562P	2.0

Date: Monday, April 10, 2017 Sheet 28 of 52

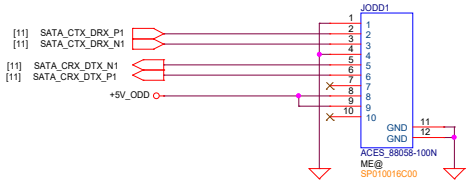
HDD

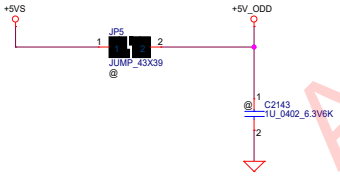
SATA HDD Conn.



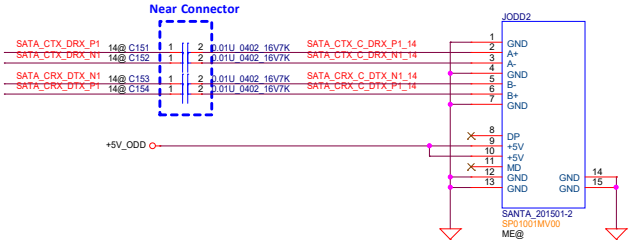
ODD

FOR 15" SATA ODD FFC Conn.





FOR 14" SATA ODD Conn.

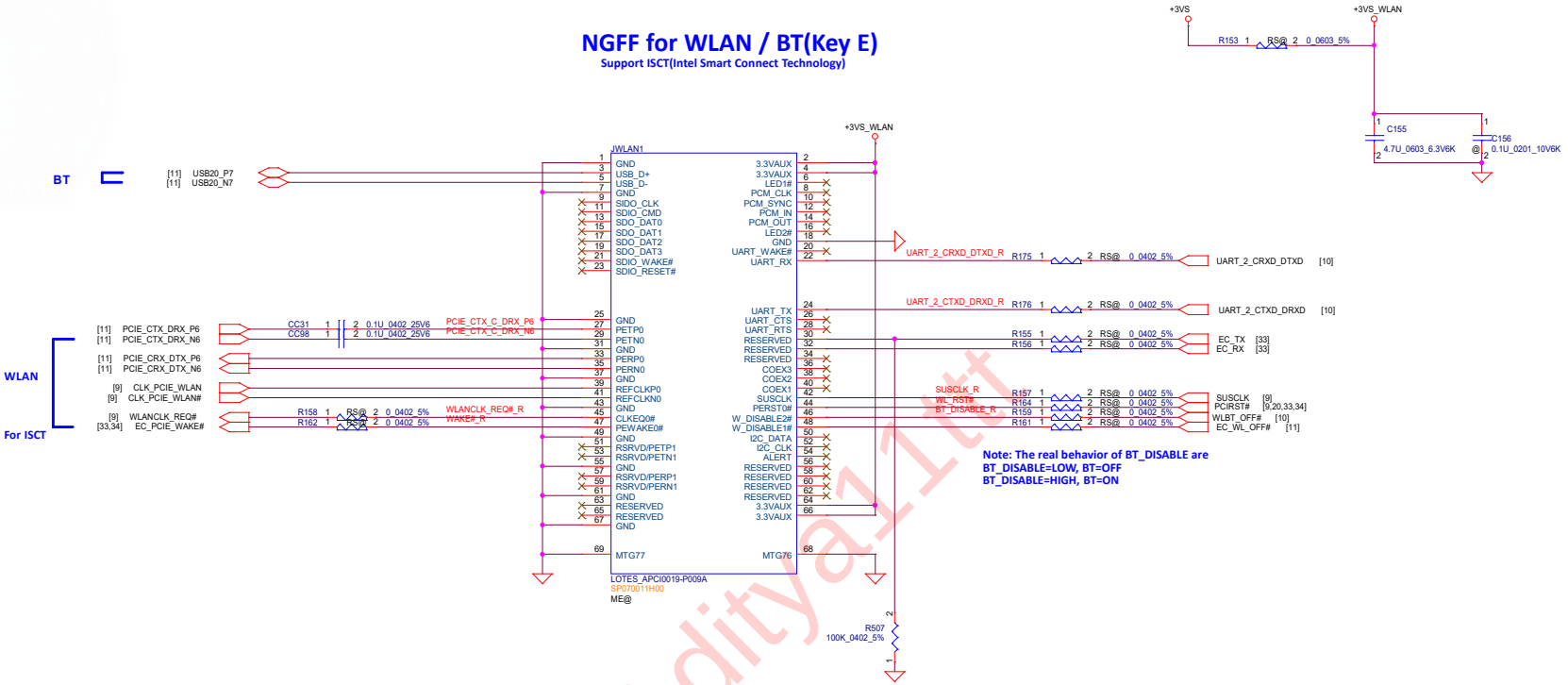


Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title: HDD/ODD Connector			
Size: C	Document Number: LA-D562P		Rev: 2.0
Date: Monday, April 10, 2017	Sheet 29 of 52		

NGFF for WLAN / BT(Key E)

Support ISCT(Intel Smart Connect Technology)



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: NGFF CARD

Size	Document Number	Rev
	LA-D562P	2.0

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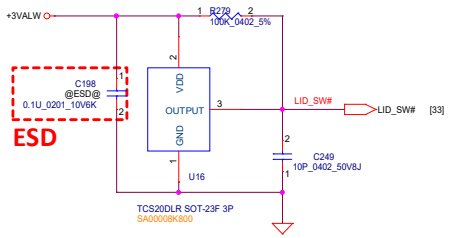
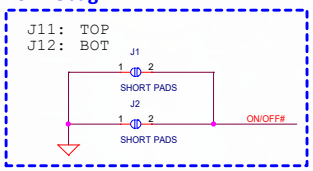
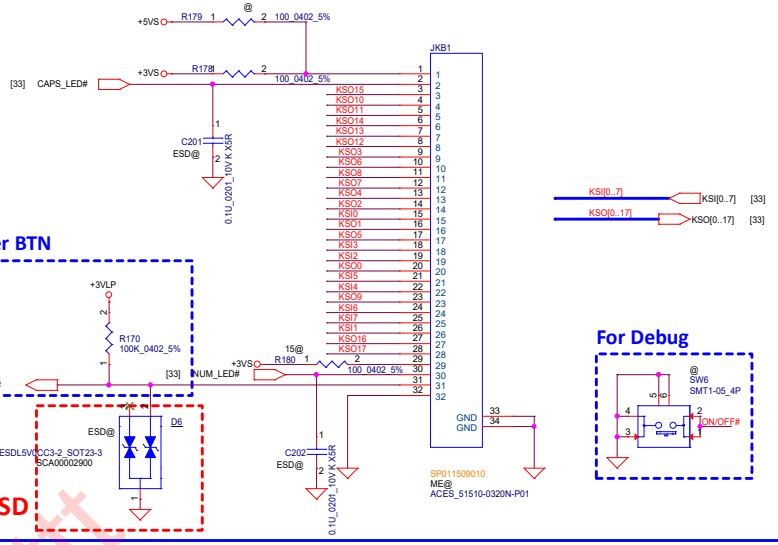
Lid switch



For Debug

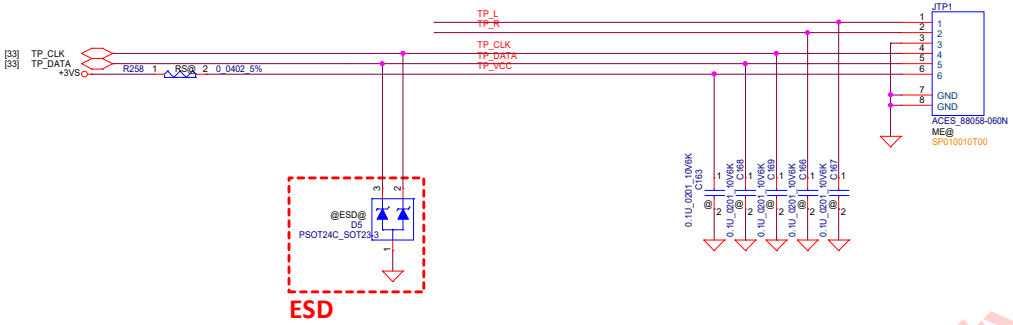


KB

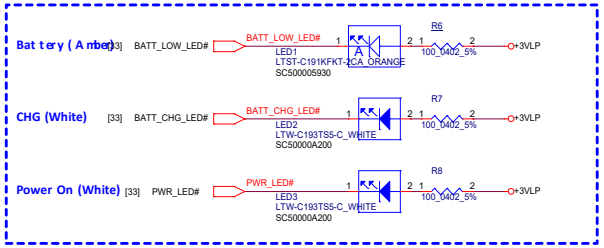


KB Power BTN

For Debug

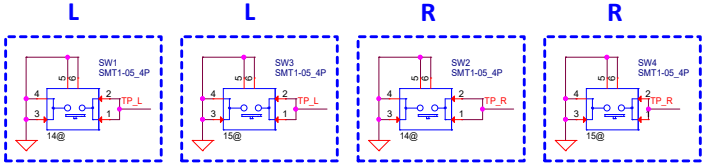


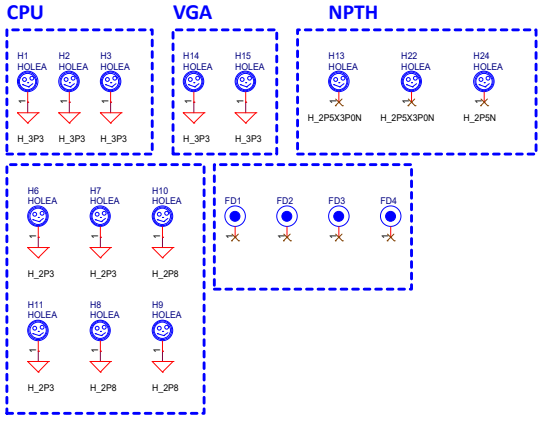
LED



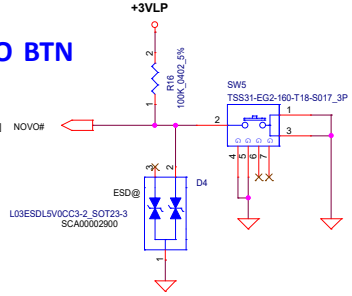
For TP module

1	1	L
2	2	R
3	3	GND
4	4	CLK
5	5	DAT
6	6	VCC

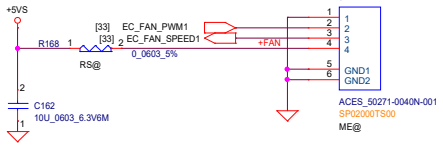




NOVO BTN

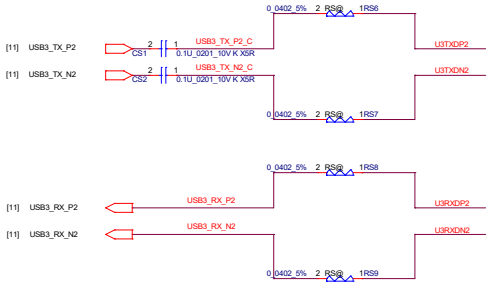


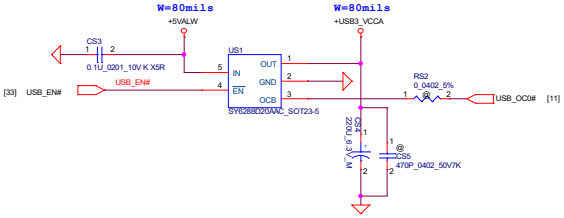
FAN Conn

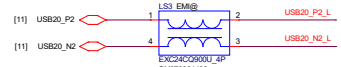


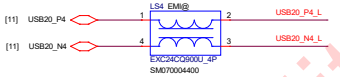
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

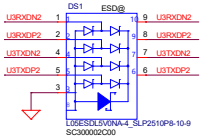
Compal Electronics, Inc.			
Title	ROM/KBD/PWR/CR/LED/TP Conn.		
Size C	Document Number LA-D562P		Rev 2.0
Date: Monday, April 10, 2017	Sheet 31 of 52		





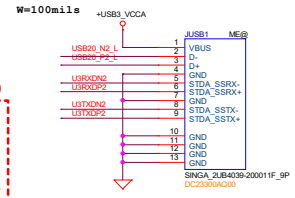




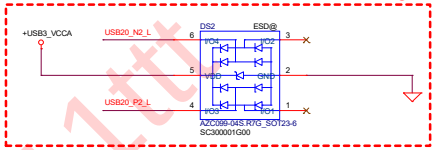


USB3.0_Port

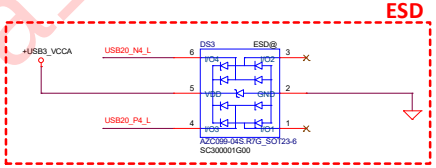
SF000002Y00
220U 6.3V OSCON
ESR 17mohm@100Khz



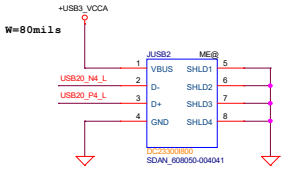
ESD



ESD

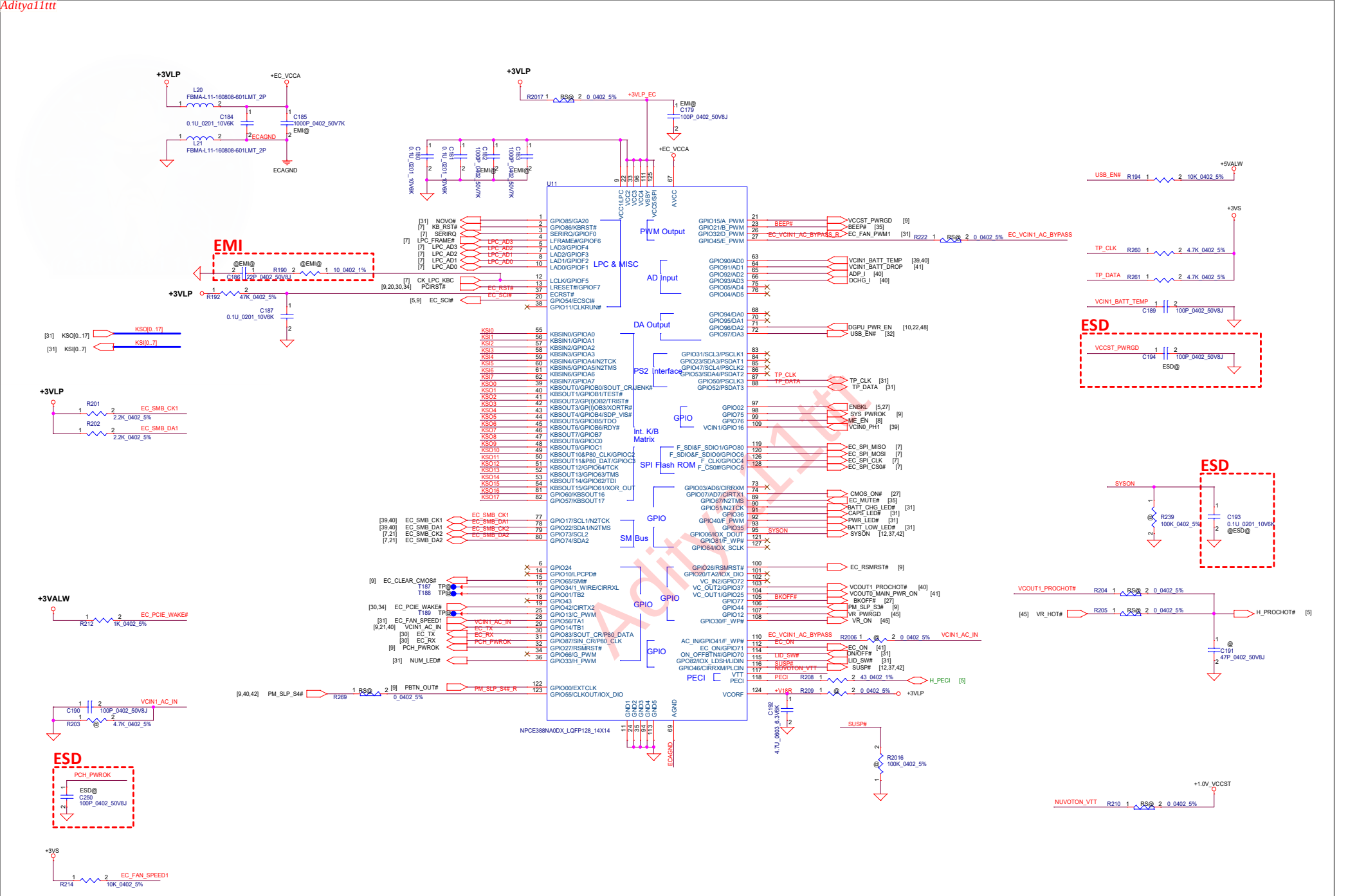


USB2.0_Port



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: SKL-U(7/12)PCIE,USB,SATA			
Size: Custom	Document Number: LA-D562P		Rev: 2.0
Date: Monday, April 10, 2017	Sheet 32 of 52		



Security Classification	Compal Secret Data		
Issued Date	2014/09/01	Deciphered Date	2015/09/01

Compal Electronics, Inc.	
Title	EC_NPCE388N
Size	C
Document Number	LA-D562P
Rev	2.0
Date:	Monday, April 10, 2017
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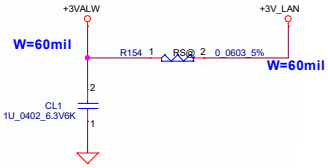
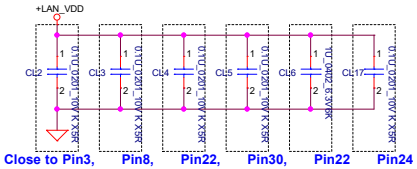
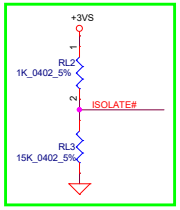
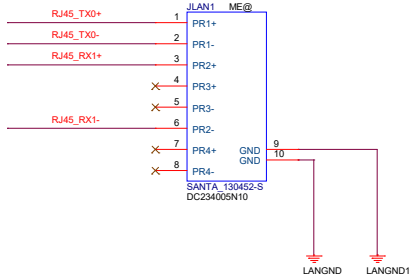
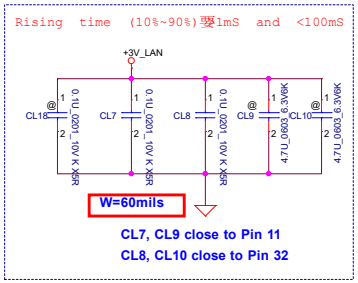
RJ-45 CONN.

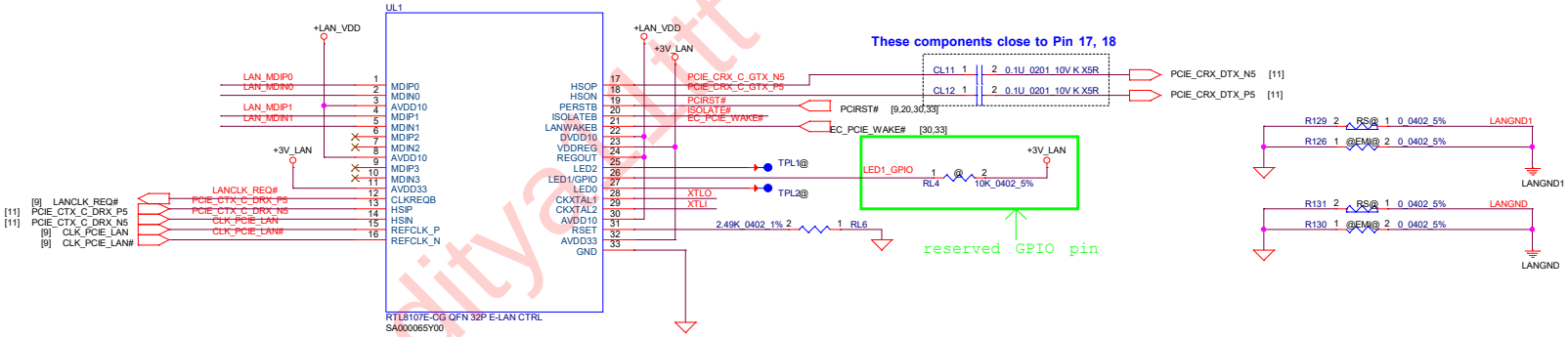




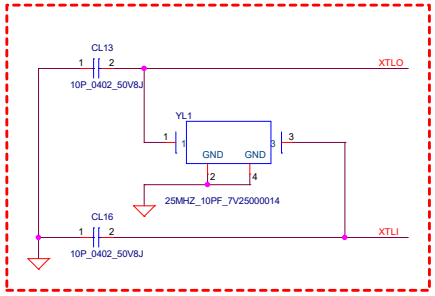




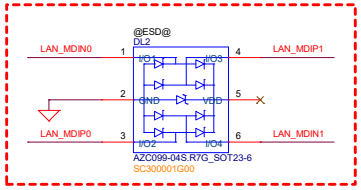


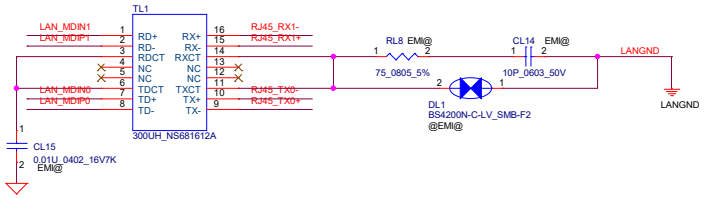


25MHz CRYSTAL



ESD





Security Classification	Compal Secret Data		
Issued Date	2013/04/12	Deciphered Date	2014/04/12

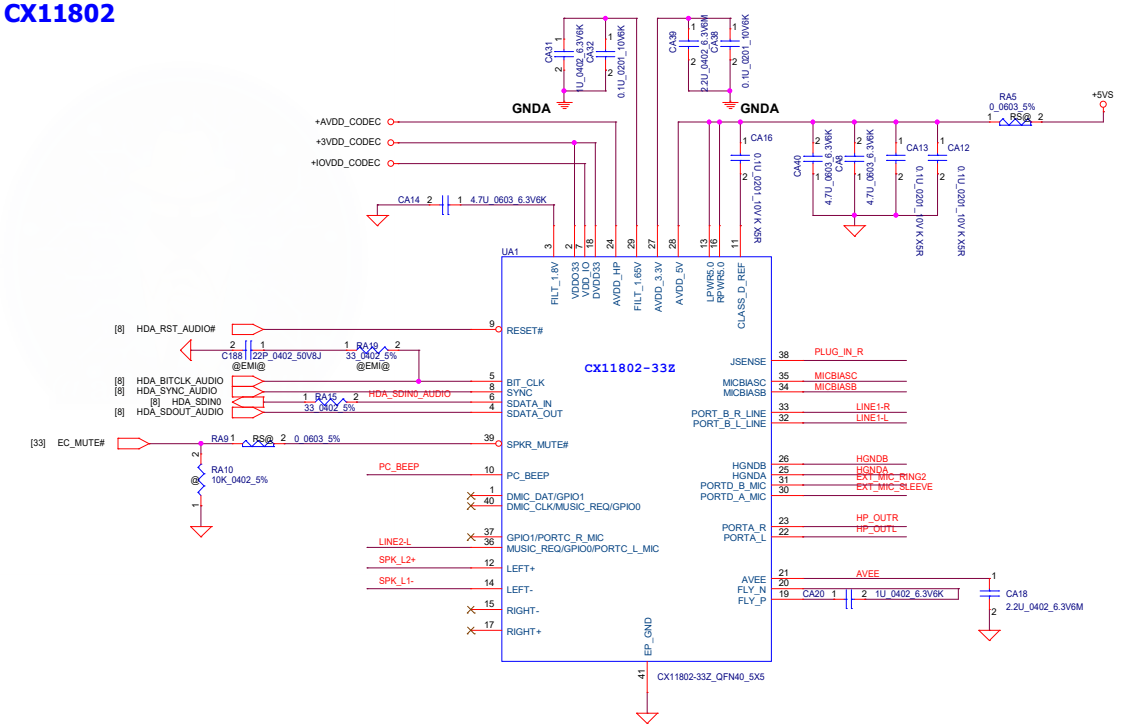
Compal Electronics, Inc.

Title: LAN RTL8107E

Size	Document Number	Rev
Custom	LA-D562P	2.0

Date: Monday, April 10, 2017 Sheet 34 of 52

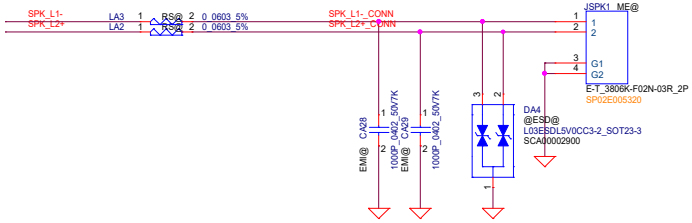
CX11802



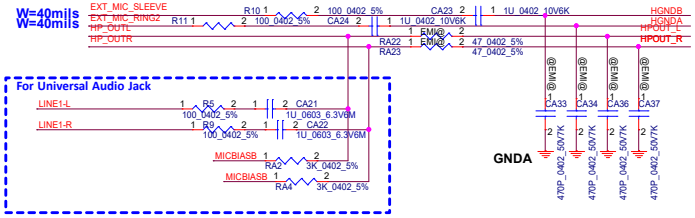
Speaker

wide 40MIL

EMI

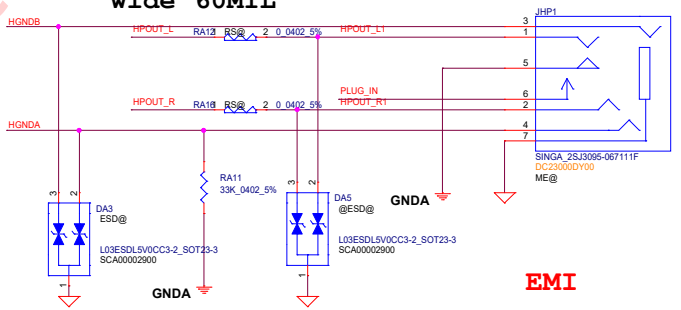


Combo Jack

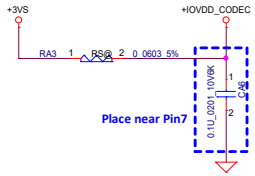


Combo Jack (Normal Open)

wide 60MIL



+3VS → +IOVDD_CODEC



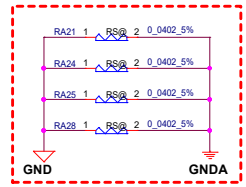
Each Platform Power Net Support List:

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
AMD Carrizo	V	V	V	V	V
AMD Carrizo-L	V	V	V	V	V
Intel Broadwell	V		V	V	V
Intel Braswell	V	V	V	V	V
Intel Skylake	V	V	V	V	V
Intel Bay trail-M	V	V	V	V	V

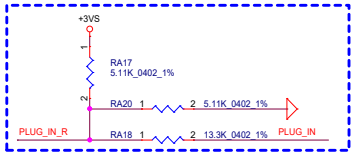
Each Platform HDA Link Voltage Support (Pin 7):

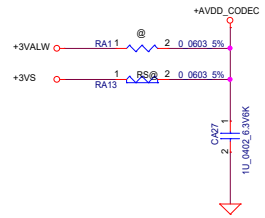
	3.3V	1.5V/1.8V
AMD Carrizo		V
AMD Carrizo-L		V
Intel Broadwell	V	V
Intel Braswell		V
Intel Skylake	V	V
Intel Bay trail-M		V

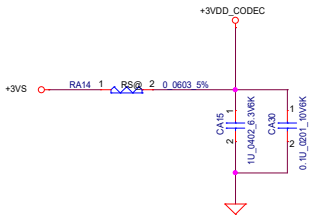
EMI



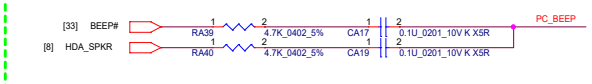
place close audio codec



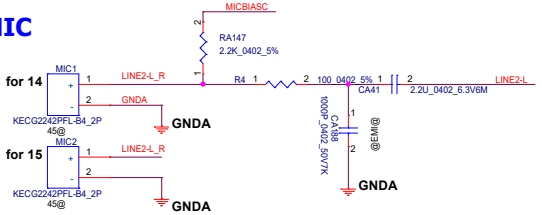




PC Beep



AMIC



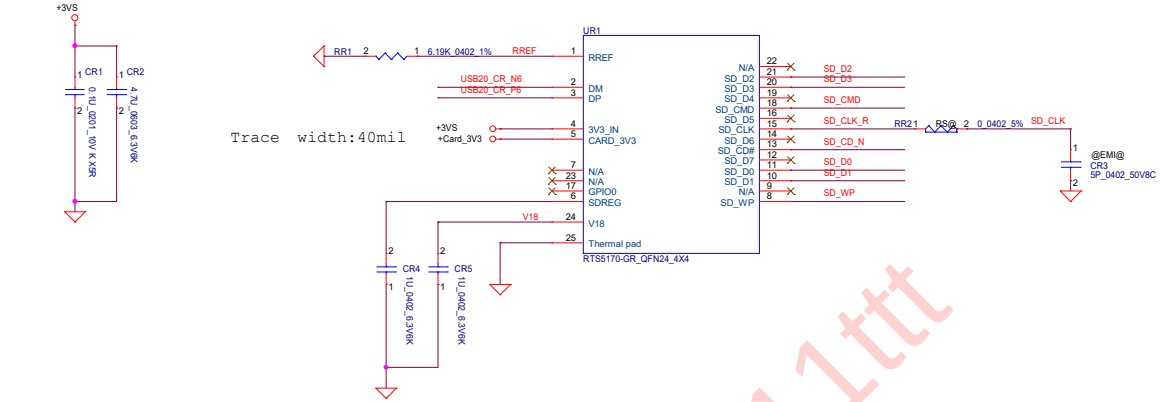
Security Classification	Compal Secret Data		
Issued Date	2014/09/01	Deciphered Date	2015/09/01

Compal Electronics, Inc.

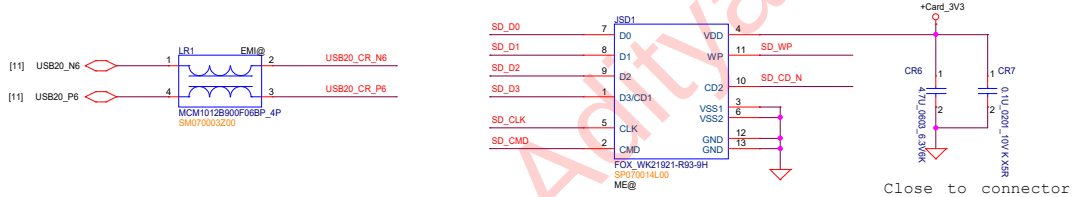
Title: HD Audio Codec_Conexant_11802

Size	Document Number	Rev
C	LA-D562P	2.0

Date: Monday, April 10, 2017 Sheet 35 of 52



SD/SDXC



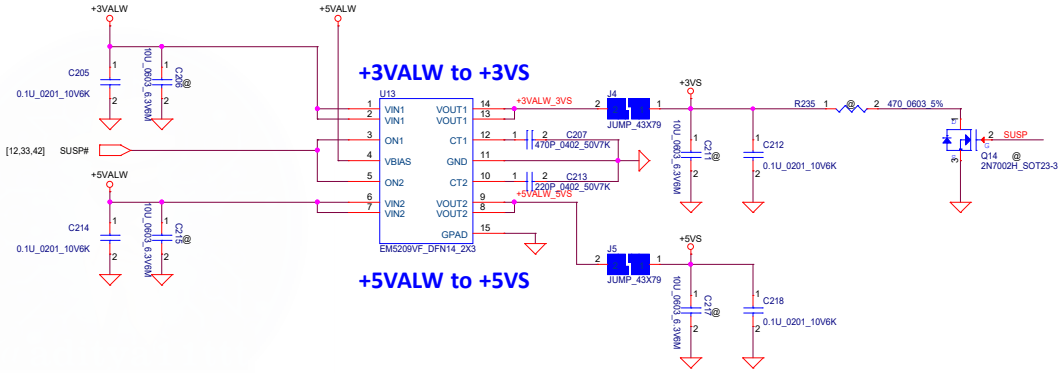
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

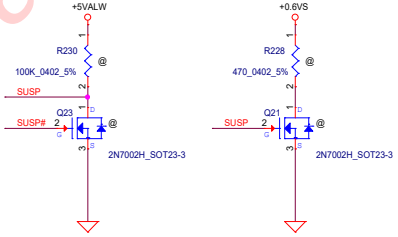
Compal Electronics, Inc.

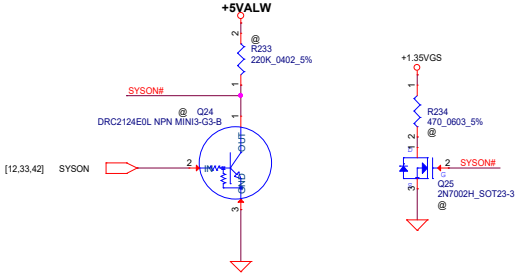
Title: CardRead/RTS5170

Size	Document Number	Rev
C	LA-D562P	2.0

Date: Monday, April 10, 2017 Sheet 36 of 52







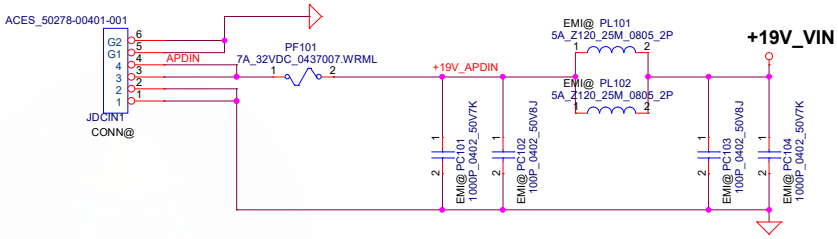
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

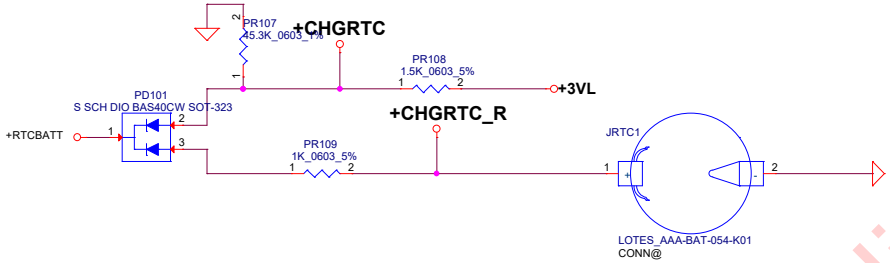
Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
C	LA-D562P	2.0

Date: Monday, April 10, 2017 Sheet 37 of 52





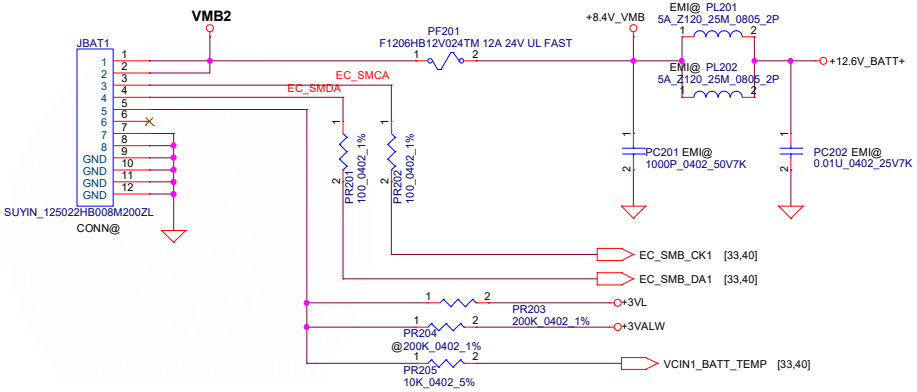
Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

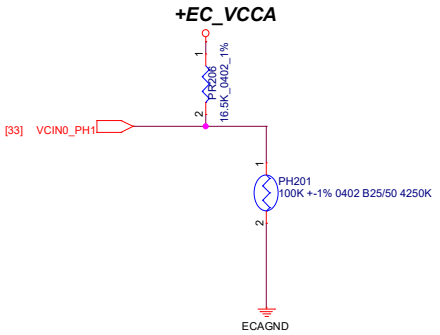
Title: **PWR- DCIN / Vin Detector**

Size	Document Number	Rev
Custom	SKL	2.0

Date: Monday, April 10, 2017 Sheet 38 of 52



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: **PWR- BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	SKL	2.0

Date: Monday, April 10, 2017 Sheet 39 of 52

<0x79> PSYS current gain
Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 10mΩ and Rs2 = 10mΩ
BIT0 = 1.14uA/W
BIT1 = 0.285uA/W
==========
Rs1 = 20mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ
BIT0 = 2.28uA/W
BIT1 = 0.57uA/W

Ipsys = KPSYS x (VADP x IADP + VBAT x IBAT)
R_Psys = 1.2V / Ipsys
KPSYS = 1.14uA/W
adapter wattage = 45W
Battery wattage = 40Wh
Ipsys = 1.14 x (45+40) = 96.9uA
R_Psys = 1.2V / 96.9uA = 12.3K-ohm.
==========
adapter wattage = 65W
Battery wattage = 40Wh
Ipsys = 1.14 x (65+40) = 119.7uA
R_Psys = 1.2V / 96.9uA = 10K-ohm.

Design Notes
For 45W/65W /90W system, 2S/3S/4S battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W
#Register Setting
1. 0X3DH bit10 set 0 (default 1) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ACLIM and CCLIM are devider voltage control.
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. SMBus timeout : 0X3DH bit15 set 0 (default 0) to enable 175s(default).
3. ACOC : OX3CH bit4 set1 release adapter limit function (default:Enable).
4. CHGOCP : based on charge current setting
5. BATOVP : 4.6V/Cell
6. BATLOWV : No.
7. TSHUT : 150C

Protection for reverse input

Vgs = 20V
Vds = 60V
Id = 250mA

PQ301 L2N7002WT1G_SC70-3
PR301 1M_0402_1%
PR302 3M_0402_5%

Rds(on) = 15.8mohm max
Vgs = 20V
Vds = 30V
ID = 10.5A (Ta=70C)

max Power loss 0.22W for 90W;0.12W for 65W system;0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV

Need check the SOA for inrush

PQ302 MDU1512RH_POWERDFN56-8-5
PQ303 AON7506_DFN33-8-5
+19V_VIN
+19V_P1
+19V_P2
PR303 0.01_1206_1%
PJP301 JUMP_43X79
+19VB_CHG
B+
PC220 10U_0805_25V6K
PC204 10U_0805_25V6K
PC205 @EMI@ 0.1U_0402_25V7K
PC206 EMI@ 2200P_0402_25V7K

Module model information
ISL95520_Hybrid_Boost_V2.mdd

Co-lay jump and ISN choke.

PR304 @ 0_0402_5%
PR305 2_0402_5%
CSIP_CHG_R
CSIN_CHG_R
PC207 0.1U_0402_25V6
PR306 392K_0402_1%
ASGATE_CHG_R
PR307 4.02K_0402_1%
PR308 4.02K_0402_1%

PR729 and PR732 are ACDET set ting base on your project to set

PR309 100_0402_1%
+12.6V_BATT+
PQ304 AON7506_DFN33-8-5
Rds(on) = 32mohm max
Vgs = 20V
Vds = 30V
ID = 8A (Ta=70C)
@PC210 0.1U_0402_25V7K

PR310 49.9K_0402_1%
PC208 2200P_0402_50V7K
support Turbo boost : 2200P
no support Turbo boost : 0.1u

CMSRC_CHG
ASGATE_CHG
PC209 0.22U_0402_16V7K
CSIP_CHG
CSIN_CHG
OPCN_CHG
OPCP_CHG
VBAT_CHG
BGATE_CHG
VDD_CHG
ACIN_CHG

PU301 ISL88739HRZ-T QFN 32P CHARGER
ACIN
ACOK
SDA
SCL
PROCHOT#
AMON
BMON
PSYS
AGND
PROG
COMP
CCLIM
FSET
BATGONE
CSON
CSOP
ACLIM
BOOT
UGATE
PHASE
LGATE
VDDP
VDD
DCIN
NTC
BST_CHG
UG_CHG
LX_CHG
LG_CHG
VDDP_CHG
VDD_CHG

PR311 100K_0402_1%
PR314 158K_0402_1%
[9,21,33] VCIN1_AC_IN
[33,39] EC_SMB_DA1
[33,39] EC_SMB_CK1
@PR313 0_0402_5%
@PR320 0_0402_5%
[33] ADP_I
[33] DCHG_I
[45] PMON_SKYLAKE
@PR318 0_0402_5%
@PR321 0_0402_5%
AMON_ISL95520
BMON_ISL95520
PC218 1000P_0402_25V8J
PC219 1000P_0402_25V8J
Close to EC
PR326 0_0402_5% @
[33] VCOUT1_PROCHOT#
PR322 @ 10K_0402_1%

Follow adapter and battery wattage in Vsys current source Base on CPU Core VR design. The resistor is pop on CPU VR schematic.

PR312 0_0603_5%
PC211 0.22U_0603_25V7K
PQ305 AON7408L_DFN8-5
7X7X3
Isat: 6.5A
DCR: 28mohm
PL302 4.7UH_5.5A_20%_7X7X3_M
+17.4V_BATT_CHG
PR315 0.01_1206_1%
+12.6V_BATT+

Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VCSPP-VCSON spec < 81mV

PR319 4.7_0402_5%
PC215 1U_0402_16V6K
PC216 1U_0402_16V6K
PQ306 AON7762_DFN3X3EP8-5
PR317 @EMI@ 4.7_1206_5%
PC217 @EMI@ 680P_0603_50V7K
PC212 10U_0805_25V6K
PC213 10U_0805_25V6K
PC214 10U_0805_25V6K

PR323 100K_0402_1%
PR324 10_1206_5%
PD102 LRB715FT1G_SOT323-3
VF = 0.38V
+19V_VIN
PC220 1U_0603_25V6
@PR316 0_0603_5%
+12.6V_BATT+
@PR339 0_0603_5%
BA
A31 connect to BA
Other team connect to bat t conn

PQ307 LMUN5113T1G_SOT323-3
[9,33,42] PM_SLP_S4#
PQ308 LMUN5236T1G NPN SOT323-3
BA

For A31 only.
Turn off Charger IC on battery only.
Depend on customer design for system power consumption.

VDD=5V
PR328 200K_0402_1%
PR329 200K_0402_1%
CCLIM_CHG
ACLIM_CHG
PROG_CHG
COMP_CHG
FSET_CHG
BATGONE_CHG
CSOP_CHG
CSON_CHG
PR325 10K_0402_1%
PR331 2_0402_5%
PC221 0.1U_0402_25V6
CSOP_CHG_R
CSON_CHG_R
@PR336 0_0402_5%

Fs=729KHZ ~ +/- 15%

@PR332 76.8K_0402_1%
@PQ310 VCIN1_AC_N
L2N7002WT1G_SC70-3
PR337 63.6K_0402_1%
U45S@
PR338 82.5K_0402_1%
PR335 150K_0402_1%
<BOM Structure>
@PR334 0_0402_5%
@PC222 560P_0402_50V7K
PR333 100_0402_1%
PC223 0.022U_0402_25V7K
VCIN1_BATT_TEMP [33,39]
BATGONE(BATT_TEMP)
logic high: above 2.4V
logic low: under 0.8V
Hybrid boost power mode
Cell = 4s
PC224 10P_0402_25V8J

(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ)
CC_LIM = VccLIM / 64 x Rs2
==========
(Rs1 = 10mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ)
CC_LIM = VccLIM / 32 x Rs2
==========
AC_LIM = Vac_LIM / 32 x Rs1

PR337 U65W@ 76.8k_0402_1%

Adapter current limimed:
For U22(45W)_adp:
PR337=53.6k
For U23e(65W) and DIS_adp:
PR337=76.8k

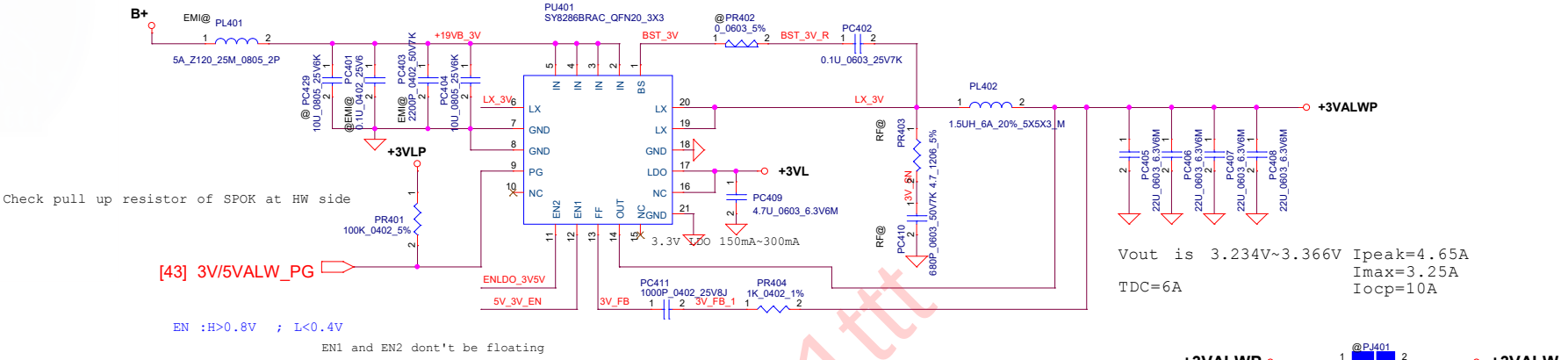
Battery current limimed by CCLIm ~ 3.89A.
Adapter current limimed by ACLIm ~ 4.33A.
(PR779 and PQ741 are for change ACLIm when AC in)

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.		
Title: PWR_CHARGER		
Size	Document Number	Rev 2.0
Date: Monday, April 10, 2017	Sheet 40 of 52	

Module model information

SY8286B_V1.mdd

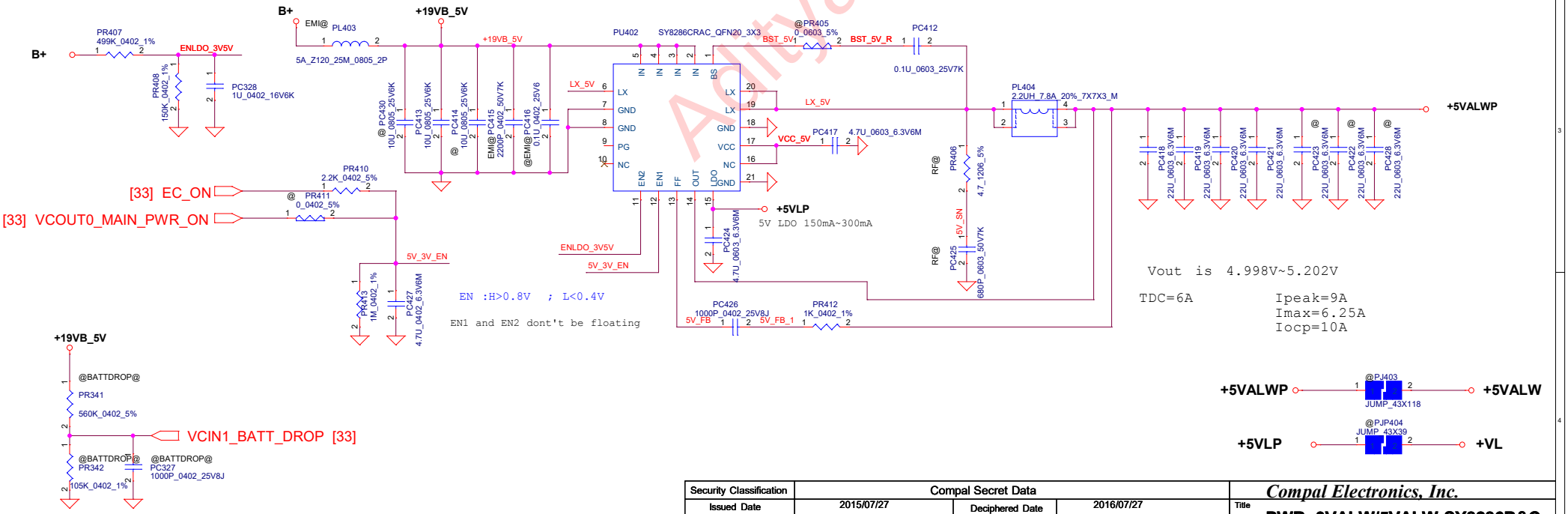


+3VALWP — @PJ401 JUMP_43X118 — +3VALW

+3VL — @PJP402 JUMP_43X39 — +3VLP

Module model information

SY8286C_V1.mdd



+5VALWP — @PJ403 JUMP_43X118 — +5VALW

+5VLP — @PJP404 JUMP_43X39 — +VL

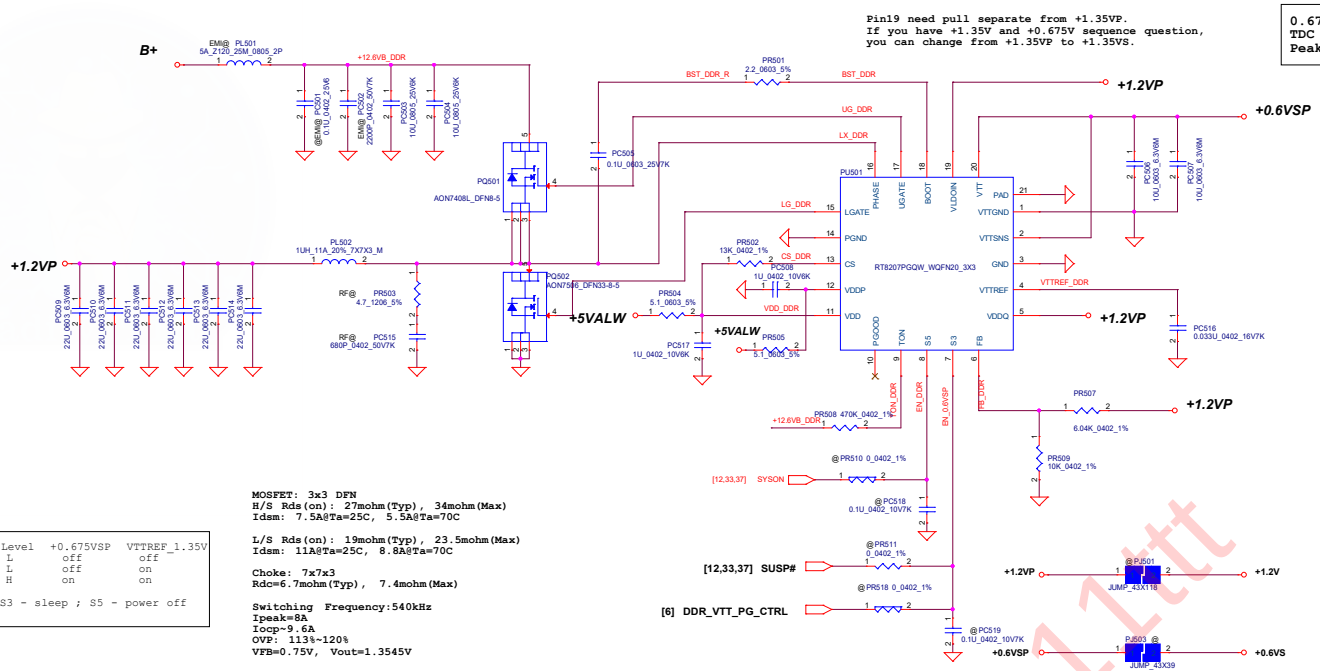
Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: PWR- 3VALW/5VALW-SY8286B&C

Size	Document Number	Rev
Custom		2.0

Date: Monday, April 10, 2017 Sheet 41 of 52



MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 19mohm(Typ), 23.5mohm(Max)
Idsm: 11A@Ta=25C, 8.8A@Ta=70C

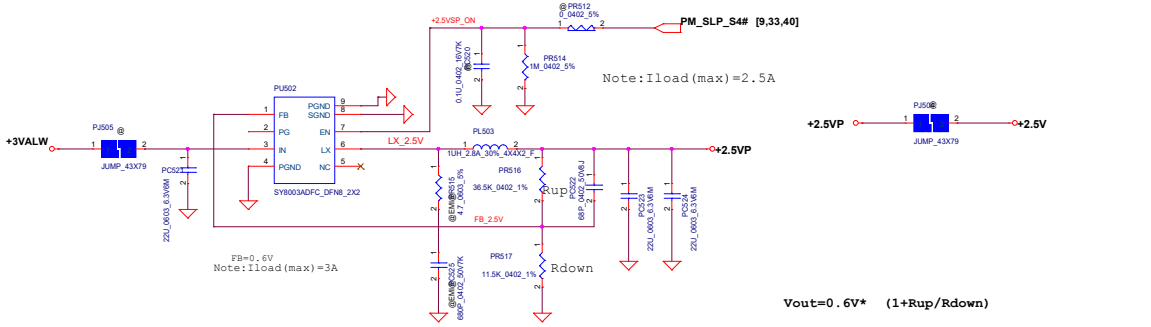
Choke: 7x7x3
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Switching Frequency:540kHz
Ipeak=8A
Iocp=9.6A
OVP: 113%~120%
VFB=0.75V, Vout=1.3545V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Module model information
SY8003A_V1.mdd



Vout=0.6V* (1+Rup/Rdown)

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

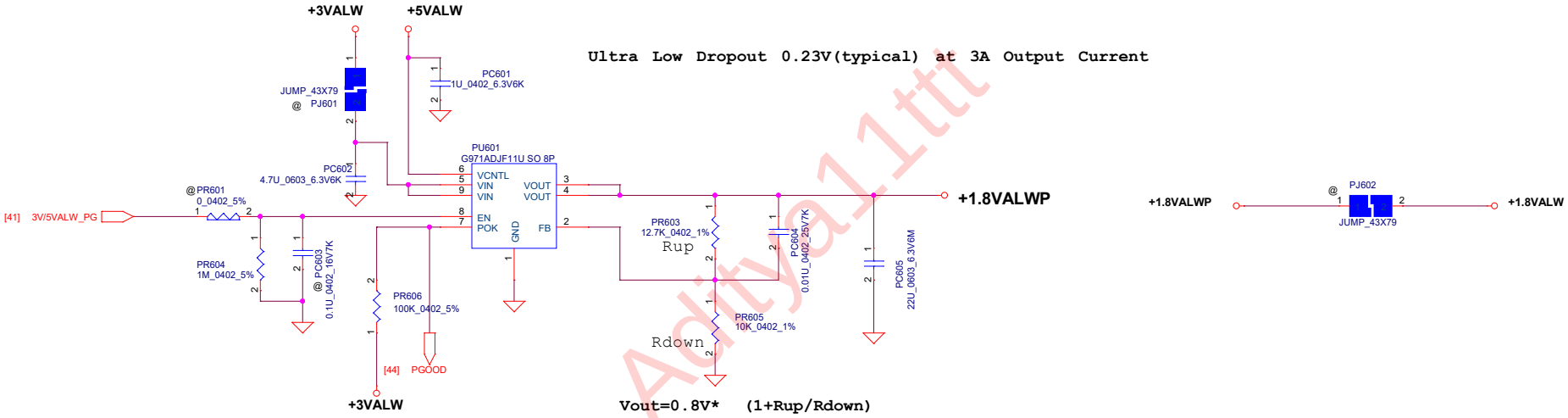
Title: +1.2VP/+0.6VSP/+2.5VP

Size	Document Number	Rev
Custom	SKL	2.0

Date: Monday, April 10, 2017 Sheet 42 of 52

Module model information

APL5930_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

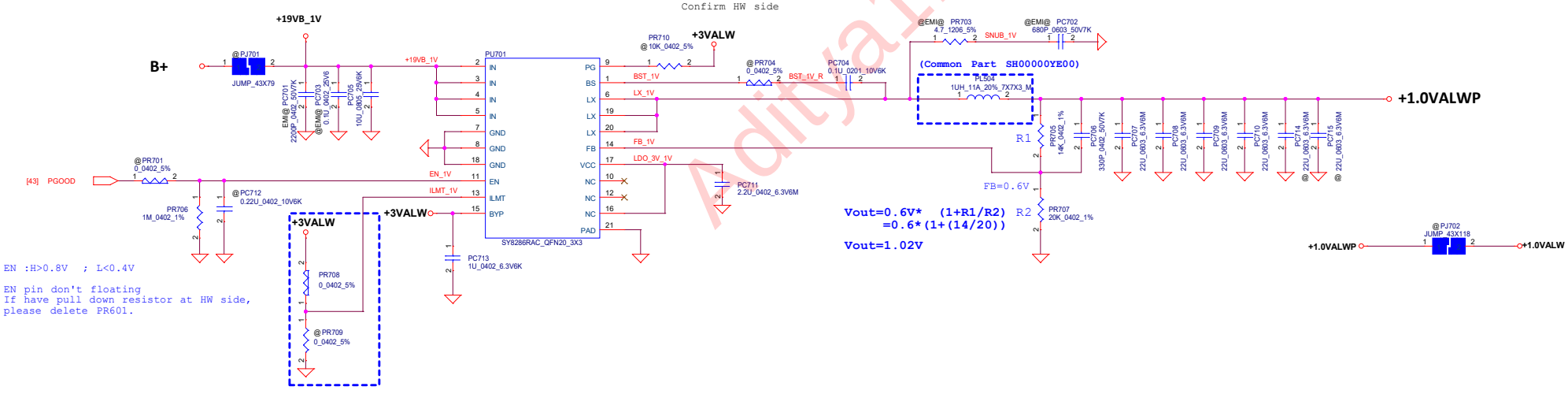
Title: +1.8V_PRIM

Size	Document Number	Rev
Custom		2.0

Date: Monday, April 10, 2017 Sheet 43 of 53

Module model information

SY8288_V1.mdd



Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: +1.0VS

Size	Document Number	Rev
C	Z_SKL	2.0

Date: Monday, April 10, 2017 Sheet 44 of 52

CPU CORE

Module model information

NCP81208_U22_V1A.mdd for IC portion

NCP81208_U22_V1B.mdd for SW portion

PSYS:
Please confirm charger pull low resistance.
Charger side should be unpop.

IccMAX@SA= 5A
RIccMAX@SA= 15.8K ---->PRI65

RIccMAX@SA= IccMAX*2V/10uA/64A

IOUTSP@SA= 5A
RIOUTSP@SA=69.8K ---->PRI14

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR /(RPHSP+Rth+RCSSP))

OCP@SA= 9.5A
RLIMSP@SA=24K ---->PRI5

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR /(RPHSP+Rth+RCSSP))

Load line@SA= 10.3m
RDRPSP@SA=1.78K ---->PRI4

RDRPSP= Load line*(RPHSP+Rth+RCSSP) /(gm * DCR) /(Rth+RCSSP)

PRI2, PRI8 place near CPU side.
If the resisters are at HW side and POP. PRI2, PRI8 can be canceled.

PRI11, PRI16 place near CPU side.
If the resisters are at HW side and POP. PRI11, PRI16 can be canceled.

IMVP8_EN
Upper Threshold > 0.8V
Lower Threshold < 0.3V

confirm with power sequence, it need behind +5VS.

PRI26 and PRI33 pull high resistor are pop at the end of VR SVID.
Other VR is unpop.

Close to VGT1 choke

Close to SA choke

Close to VCORE choke

Close to VGT1 MOS

Close to VCORE MOS

OCP for VGT

OCP for VCORE

RPH@GT:

U22 OCP@GT= 40A
RLIM@GT=12.4K ---->PRI39

RLIM= IoutLIMIT * Load line/10

U22 IccMAX@GT= 31A
RIccMAX2ph= 48.7K ---->PRI63

RIccMAX2ph= (IccMAX2Ph+32)*200K Ohn/ 127

U22 Iout@GT= 31A
RIOUT@GT=25.5K ---->PRI23

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

U22 Load line@GT= 3.1m
RPH@GT=84.5K ---->PRI30,PRI38

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))
*IOUTTOTAL * DCR/RPH

472mV/120uA=3.933K
Active Point110 degreeC = 4.206K

NCP81208 Operating Frequency Rosc=33.2K
I/A and GT are 450KHz
NCP81208 Operating Frequency Rosc=24K
and SA is 600KHz

472mV/120uA=3.933K
Active Point110 degreeC = 4.206K

VBOOT:
2.2K for debuge setting.

PRI51, PRI58 place near CPU side.
If the resisters are at HW side and POP. PRI51, PRI58 can be canceled.

U22 Load line@VCORE= 2.35m
RDRPSP@VCORE=2.1K ---->PRI56

RDRPSP= Load line*(RPHSP+Rth+RCSSP) /(gm * DCR) /(Rth+RCSSP)

IccMAX@VCORE= 28A
RIccMAX@VCORE= 87.6K ---->PRI64

RIccMAX@VCORE= IccMAX*2V/10uA/64A

IOUTSP@VCORE= 28A
RIOUTSP@VCORE=64.9K ---->PRI42

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR /(RPHSP+Rth+RCSSP))

OCP@VCORE= 35A
RLIMSP@VCORE=33.4K ---->PRI53

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR /(RPHSP+Rth+RCSSP))

Title	NCP81208
Size	Document Number / Rev 2.0
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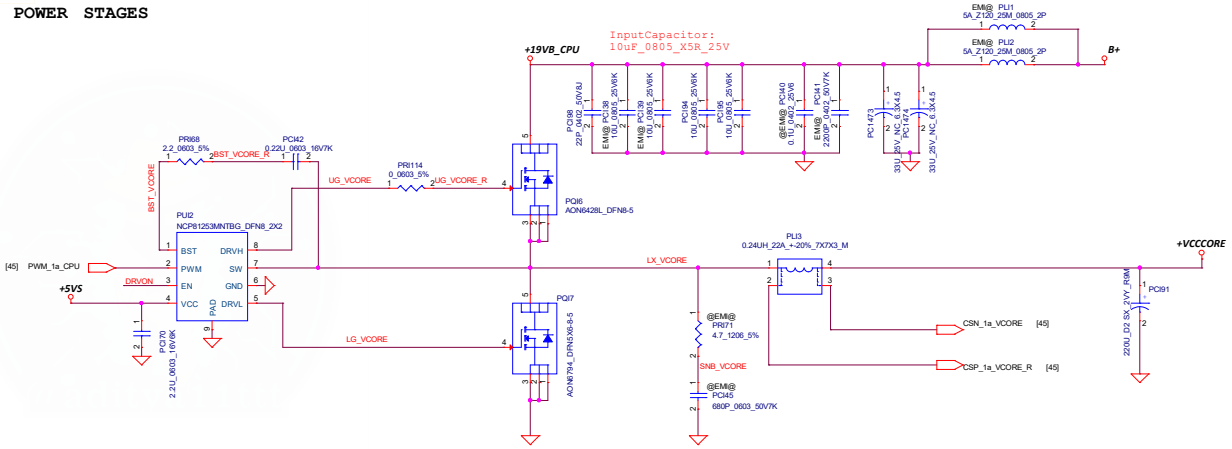
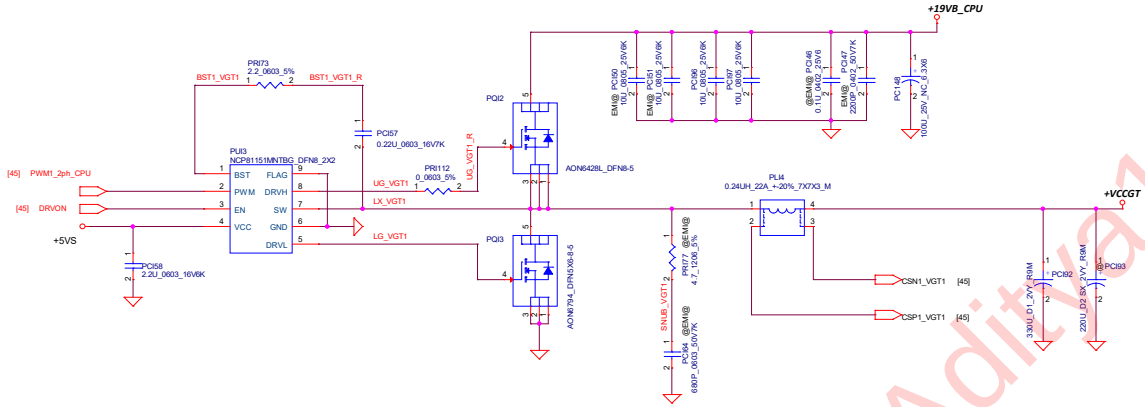
CPU POWER STAGES



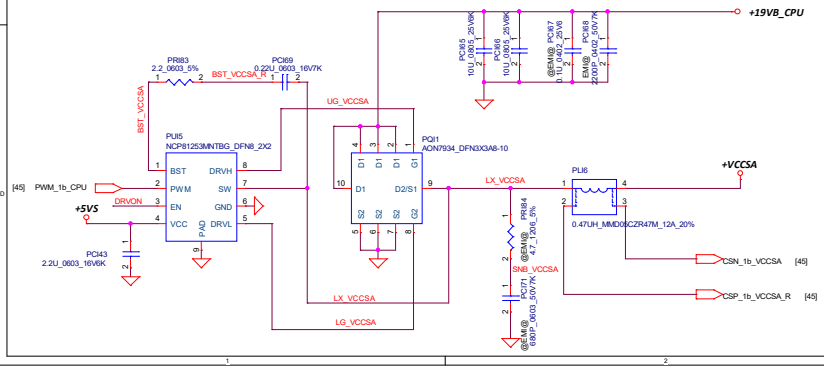
VCC_CORE
FSW=450kHz
DCR = 1.19 mohm +/- 5%

	TYP	MAX
H/S Rds(on)	:11.3mohm ,	14.5mohm
L/S Rds(on)	:2.8mohm ,	3.5mohm



VCCGT
FSW=450kHz
DCR = 1.19 mohm +/- 5%

	TYP	MAX
H/S Rds(on)	:11.3mohm ,	14.5mohm
L/S Rds(on)	:2.8mohm ,	3.5mohm



VCCSA
FSW=450kHz
DCR 6.2mohm(TYP), 6.51mohm(Max)

	TYP	MAX
H/S Rds(on)	:12.4mohm ,	15.8mohm
L/S Rds(on)	:9.1mohm ,	11.6mohm

Title	Power Stage	
Size	Document Number	Rev 2.0
Date: Monday, April 10, 2017	Sheet 46 of 52	

VCC_CORE Place on CPU Back Side @ V09
22U_0603 * 28 pcs +1U_0201*35 pcs

VCC_GT Place on CPU Back Side @ V09
22U_0603 * 29 pcs +1U_0201*12 pcs

+VCCCORE

+VCCGT

VCC_SA Place on CPU Back Side @ V09
22U_0603 * 9 (4 CPU back+8 outside)pcs + 1U_0201*7

+VCCSA

+VCCGT

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: PWR-PROCESSOR_DECOUPLING

Size	Document Number	Rev
C		2.0

Date: Monday, April 10, 2017 Sheet 47 of 52

Module model information

ISL62771_CZ_GFX35W_V1A.mdd for IC portion
ISL62771_CZ_GFX35W_V1B.mdd for SW portion

VR_ON
High > 1.6V
Low < 1V

PH1002 near APU_CORE H/S mos
VRHOT Assert Threshold : 0.64V
TSENSE Bias Current : 30uA
PH1002=27.4K, 110C active
Reset Threshold: 0.66V, 98C active
110C Assert Threshold: PR1031=27.4K
100C Assert Threshold: PR1031=16.9K

PH1003 near GFX_CORE choke

PR1046 set 750 ohm to OCP 43.75A

PR1058=3.65K, PR1040=2.1K and
PR1046=604 to set loadline -2.1mV/A

PR1058=3.65K, PR1040=2.1K and
PR1046=604 to set loadline -2.1mV/A
while PR1046=594 to set OCP 57.16A
for EDC 45A application.

SH000011H00 (DCR:0.98mohm +/-5%)

+VGA_CORE

GFX_core
TDC 28(1H1L)
Peak Current 42A
OCP current > 42A
Load line -2.1mV/A
FSW=400kHz
DCR 0.98mohm +/-5%

	TYP	MAX
H/S Rds(on)	:6.8mohm ,	8.6mohm
L/S Rds(on)	:2mohm ,	2.5mohm

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702

Confirm HW side

keep short pad, snubber is for EMI only.

(Common Part SH000002Z00)

+1.35VGSP

Vout=0.6V* (1+R1/R2)
=0.6*(1+(14/11))
Vout=1.36V

EN :H>0.8V ; L<0.4V

EN pin don't floating
If have pull down resistor at HW side,
please delete PR601.

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

Compal Electronics, Inc.

Title: PWR-CPU_CORE/CPU_CORE_NB

Size	Document Number	Rev
Custom	ISL62771 Module	2.0

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	導R17-M1-70	P49	PR1408改M170@ PR1410從-short 改M150 @ PR1428,PR145改M150 @ 糧PC141, PC145,都改為 M1 70 @ PC1417 from 150P change to 270P PR1424 M130 pop 1.37K M170 pop 1K PR1421 A phase 纔是否 p op	2016/11/3	
3					
4					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: **PIR (PWR)**

Size	Document Number	Rev
Custom	Z_BDW	2.0

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