Iris2 Schematics
Skylake-U

2015/05/20
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

Iris SKL UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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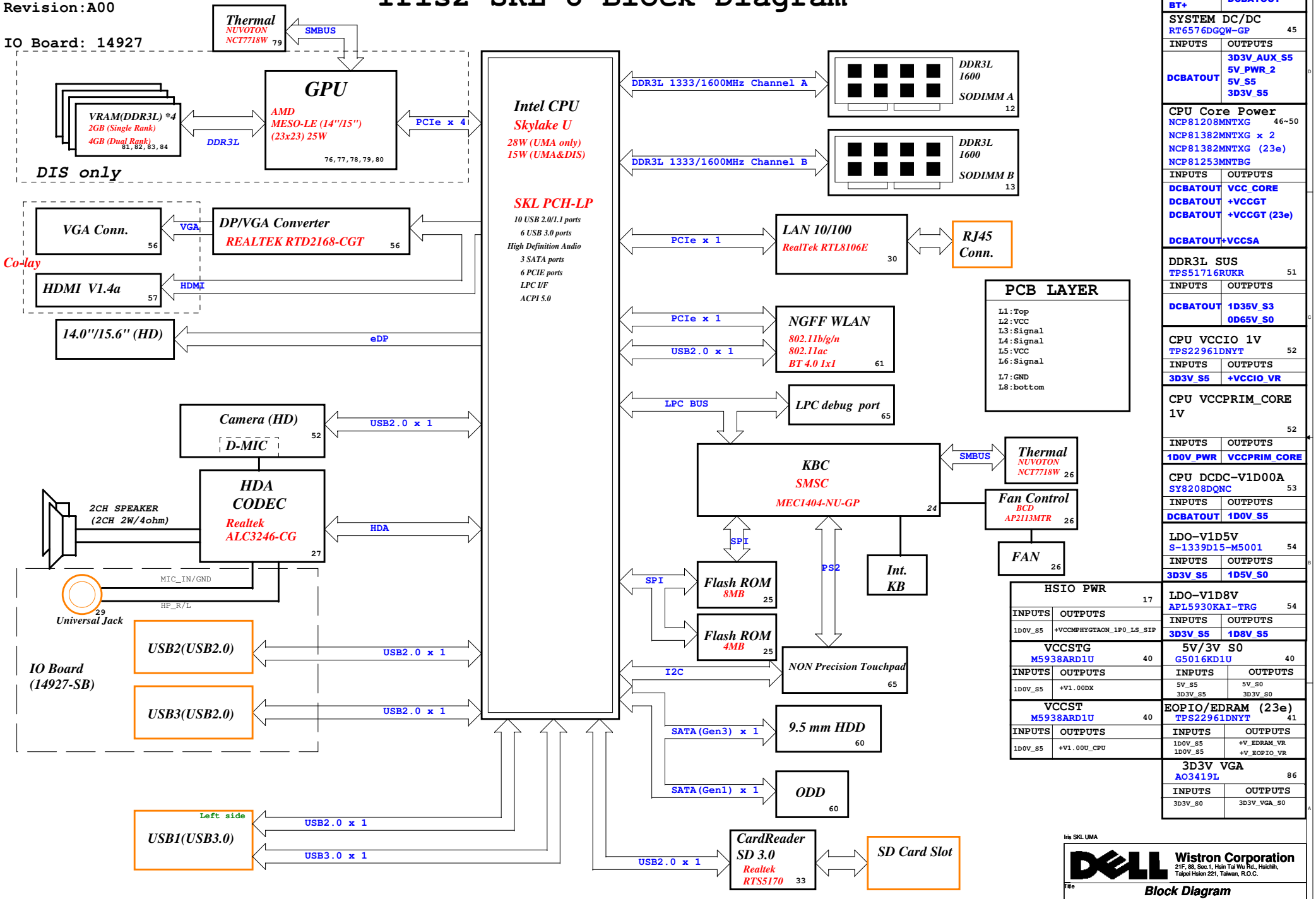
Title: *Cover Page*		
Size: A3	Document Number: Iris2 SKL-U	Rev: X02
Date: Tuesday, September 08, 2015	Sheet 1 of 105	

Project code:
Iris-2 14 --> 4PD02V010001
PCB P/N: 14236-SF
Revision:A00

IO Board: 14927

Iris2 SKL-U Block Diagram



PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:bottom

HSIO PWR 17

INPUTS	OUTPUTS
1D0V_S5	+VCCMPHYGTAON_1P0_LS_SIP

VCCSTG M5938ARD1U 40

INPUTS	OUTPUTS
1D0V_S5	+V1.00DX

VCCST M5938ARD1U 40

INPUTS	OUTPUTS
1D0V_S5	+V1.00U_CPU

CHARGER BQ24770RUYR 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT6576DGQW-GP 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_PWR_2 5V_S5 3D3V_S5

CPU Core Power NCP81208MNTXG 46~50

NCP81382MNTXG x 2
NCP81382MNTXG (23e)
NCP81253MNTBG

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT	+VCCSA

DDR3L SUS TPS51716RUKR 51

INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0

CPU VCCIO 1V TPS22961DNYT 52

INPUTS	OUTPUTS
3D3V_S5	+VCCIO_VR

CPU VCCPRIM_CORE 1V 52

INPUTS	OUTPUTS
1D0V_PWR	VCCPRIM_CORE

CPU DCDC-V1D00A SY8208DQNC 53

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D5V S-1339D15-M5001 54

INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

LDO-V1D8V APL5930KAI-TRG 54

INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0 G5016KD1U 40

INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

EOPIO/EDRAM (23e) TPS22961DNYT 41

INPUTS	OUTPUTS
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR

3D3V VGA AO3419L 86

INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0

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Title: Block Diagram

Size	Document Number	Rev
C	Iris2 SKL-U	A00

Date: Tuesday, May 26, 2015 Sheet 2 of 105

Main Func = CPU

(Blanking)

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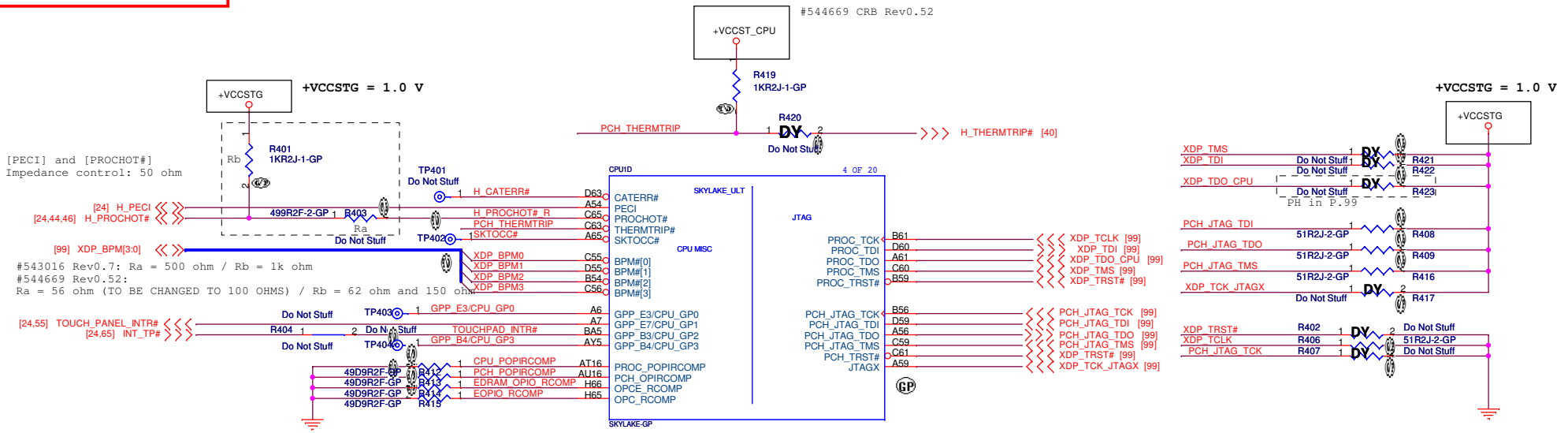
Title: (Reserved)

Size: A3 | Document Number: Iris2 SKL-U | Rev: A00

Date: Tuesday, May 26, 2015 | Sheet 3 of 105

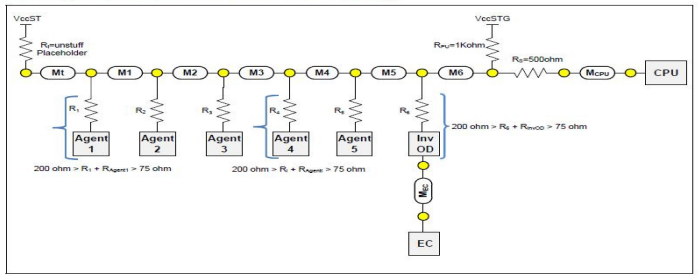
Main Func = CPU



071.SKYLA.000U

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

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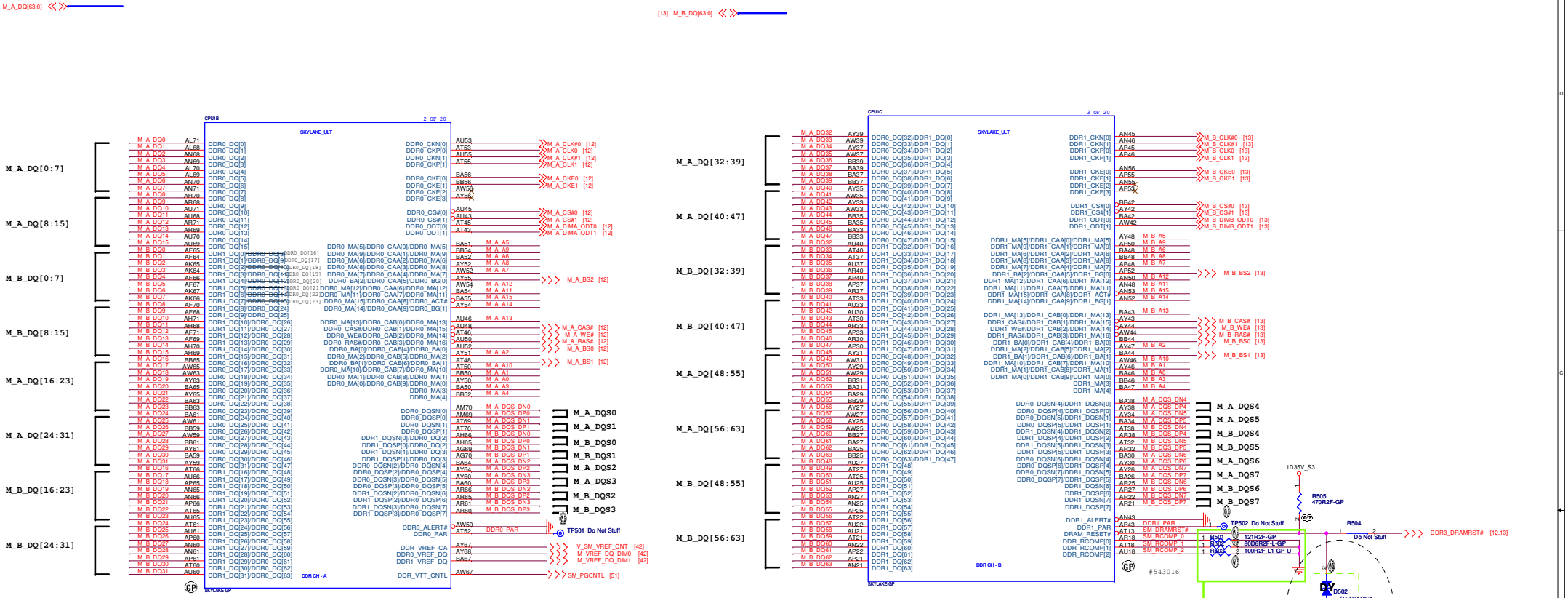
Title	CPU_(JTAG/CPU SIDE BAND)	
Size A3	Document Number Iris2 SKL-U	Rev X02
Date: Wednesday, September 09, 2015	Sheet 4 of 105	

Main Func = CPU

DDR3L ball type: Interleaved Type



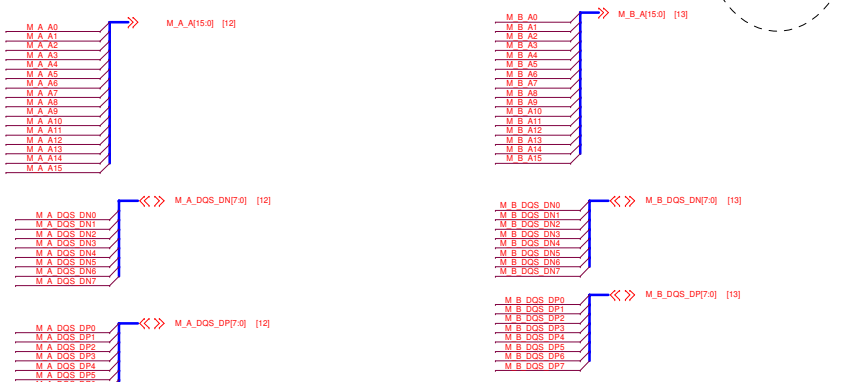
071.SKYLA.000U

071.SKYLA.000U

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

Layout Note:



PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

Processor	Memory type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0] DDR1_ODT[0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
	DDR3L Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT.	3,4
		DRAMs	ODT[1:0]	Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	
	DDR3L SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DIMMs ODT[1:0].	1,3
		DIMMs	ODT[1:0]		
	DDR3L Mixed Memory Down and SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's SODIMM Channel ODT[1:0] connected to DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If rank1 not used, ODT[1] not connected.	3,4
		DIMM	ODT[1:0]		
		DRAMs	ODT[1:0]		
	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.	
		DRAMs	ODT[1:0]		
	DDR4 SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.	
		DIMMs	ODT[1:0]		

Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP3 - SKL-Y LPDDR3, RVP5 - SKL-U LPDDR3)
2. LPDDR3 Rank1 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active), RTT NOM is defined by BIOS as High-Z in both ranks, when a Rank receives write command it enables RTT WR (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z).
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SDP dual sided and 2Rx8 dual side.

Iris SKL UMA

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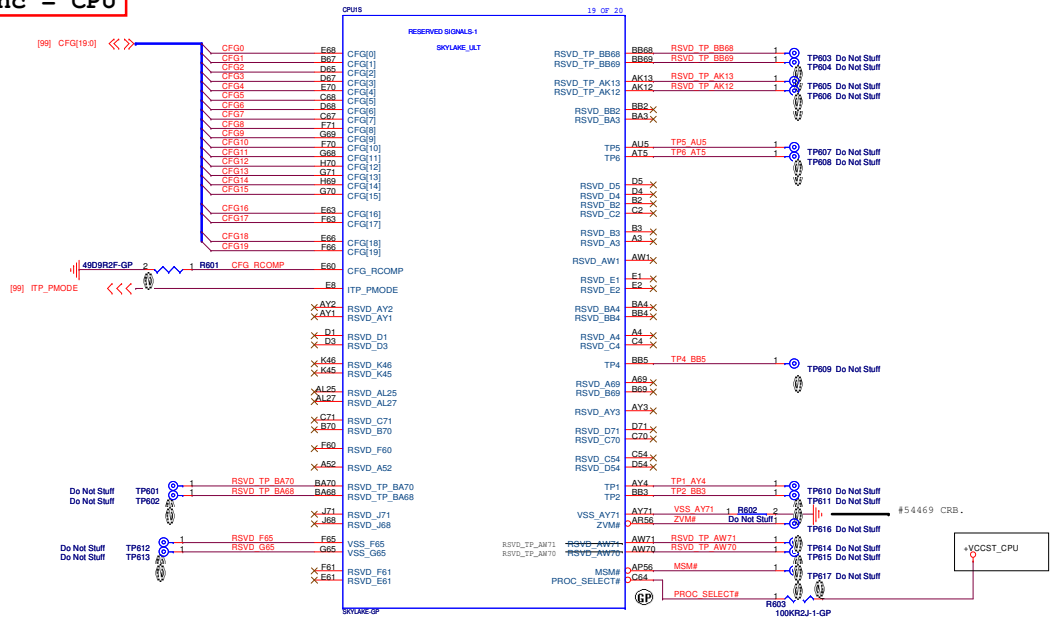
Title: CPU_(DDR)

Size	Document Number	Rev
A2	Iris2 SKL-U	A00

Date: Wednesday, September 09, 2015 Sheet 5 of 105

Main Func = CPU



CFG TERMINATIONS

#544669 Rev0.52 (CRB)

20140807 david

PCH strap pin:

071.SKYLA.000U

CFG3 — R604 Do Not Stuff

[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

(#543016)

CFG4 — R605 1KR2J-1-GP

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

SKL(#543016):

Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

Iris SKL UMA

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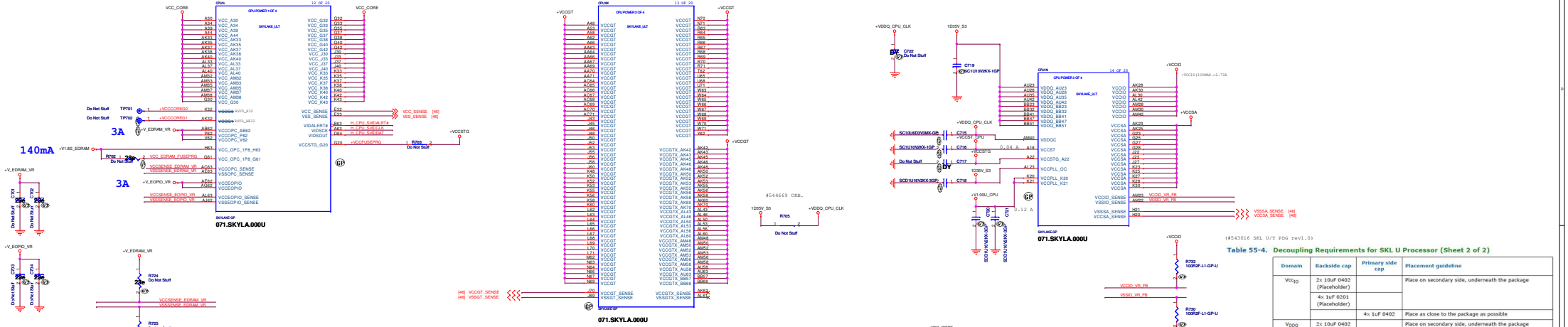
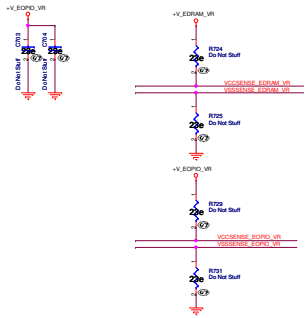
Title: CPU_(RESERVED)

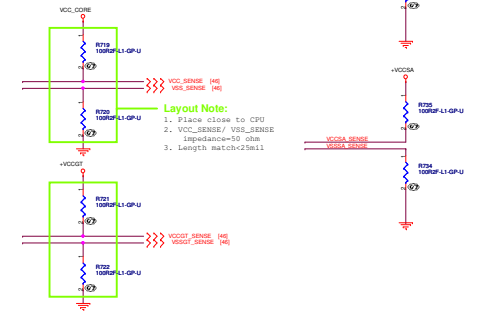
Size: A2 | Document Number: Iris2 SKL-U | Rev: A00

Date: Wednesday, September 09, 2015 | Sheet 6 of 105

Main Func = CPU







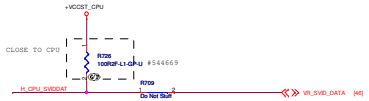
(#543016 SKL U/Y PDG rev1.0)

Table 55-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

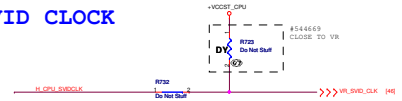
Domain	Backside cap	Primary side cap	Placement guideline
V_{CCIO}	2x 10uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1uF 0201 (Placeholder)		
		4x 1uF 0402	Place as close to the package as possible
V_{DDQ}	2x 10uF 0402 (Placeholder)		Place on secondary side, underneath the package
	4x 1uF 0201 (Placeholder)		
		4x 10uF 0402	Place as close to the package as possible
		3 x 22uF 0603	Place as close to the package as possible
V_{DDQC}	1x 1uF 0201 (Placeholder)		Place on secondary side, underneath the package
		1 x 10uF 0402	Place as close to the package as possible
V_{CCPLL}		1x 1uF 0402	Place as close to the package as possible
V_{CCPLL_OC}		1x 1uF 0201	Place as close to the package as possible
V_{CCST}		1x 1uF 0402	Place as close to the package as possible
V_{CCSTG}	1x 1uF 0402 (Placeholder)		Place on secondary side, underneath the package Placeholder only
$V_{CCEOPIO}$	2x 10uF 0402		Place on secondary side, underneath the package
V_{CCOPC}	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

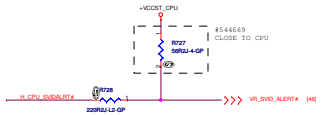
SVID DATA

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



SVID CLOCK



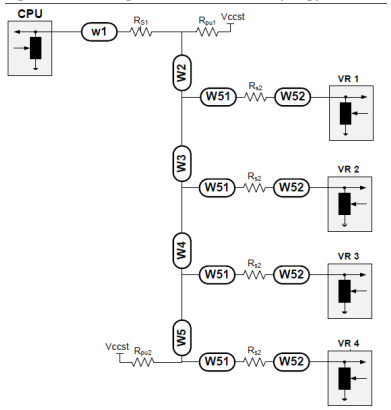


SVID_543016:

Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU0} [Ω]	R_{PU1} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	V_{CCST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Figure 10-7. Routing Illustration for SVID Topology



Ite SKL UMA

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Title: CPU(VCC_CORE)

Size	Document Number	Rev
A3	Iris2 SKL-U	A00

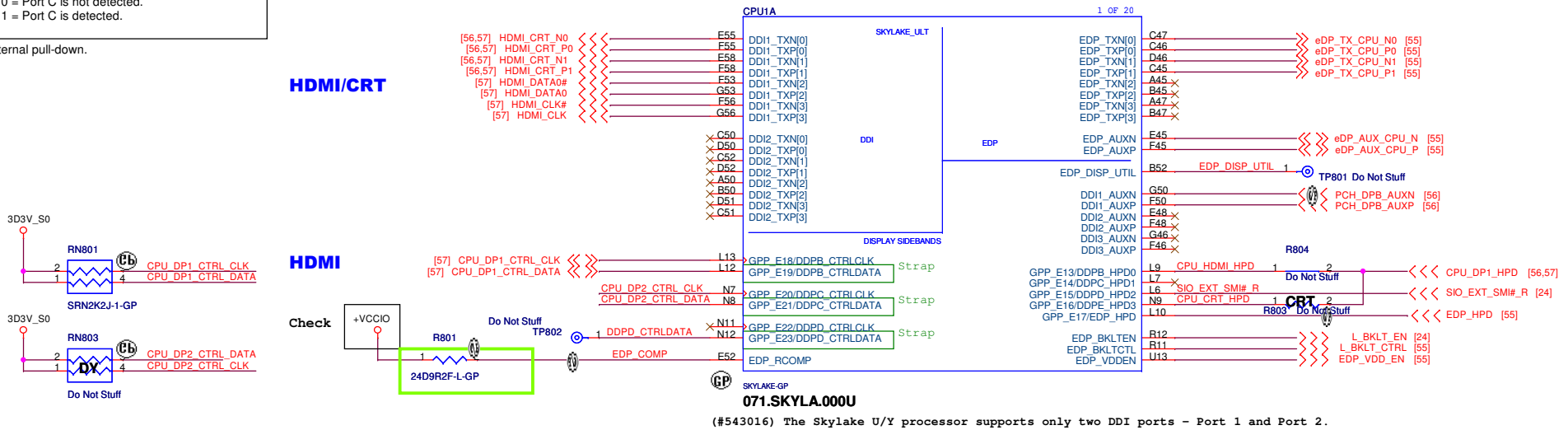
Date: Wednesday, September 02, 2015 Sheet 7 of 155

Main Func = CPU

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

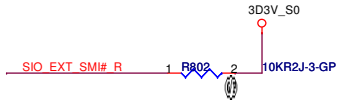
These two signals have weak internal pull-down.



(#543016) The Skylake U/Y processor supports only two DDI ports – Port 1 and Port 2.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils



(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

Iris SKL UMA

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Title: CPU_(DISPLAY)

Size: A3 | Document Number: Iris2 SKL-U | Rev: A00

Date: Wednesday, September 09, 2015 | Sheet 8 of 105

Main Func = CPU

(Blanking)

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Title: (Reserved)

Size: A3 | Document Number: Iris2 SKL-U | Rev: A00

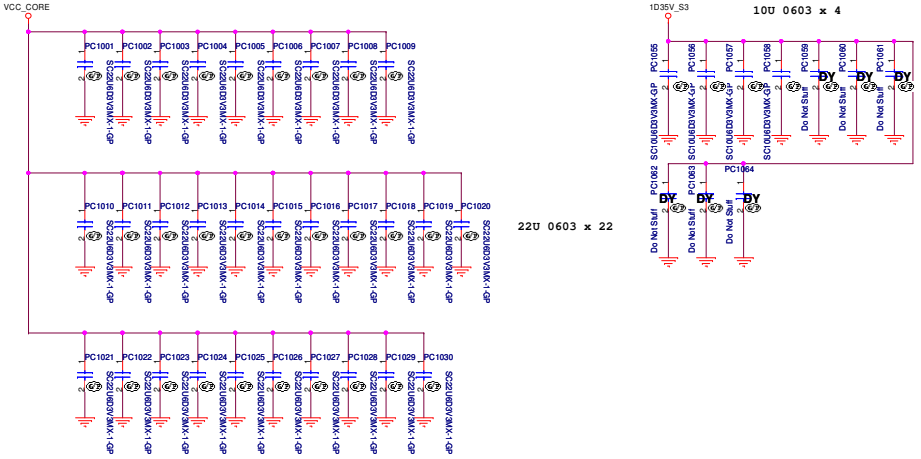
Date: Tuesday, May 26, 2015 | Sheet 9 of 105

Main Func = CPU

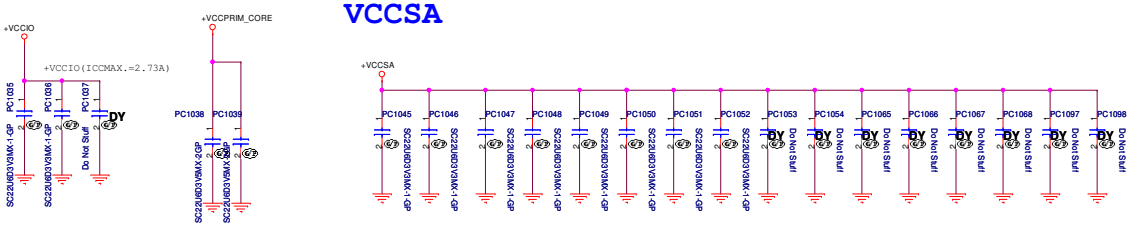
(#543016 PDG)

CORE

U-line 23e 28W
IccMax current-10ms max = 34 A



VCCSA



SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A

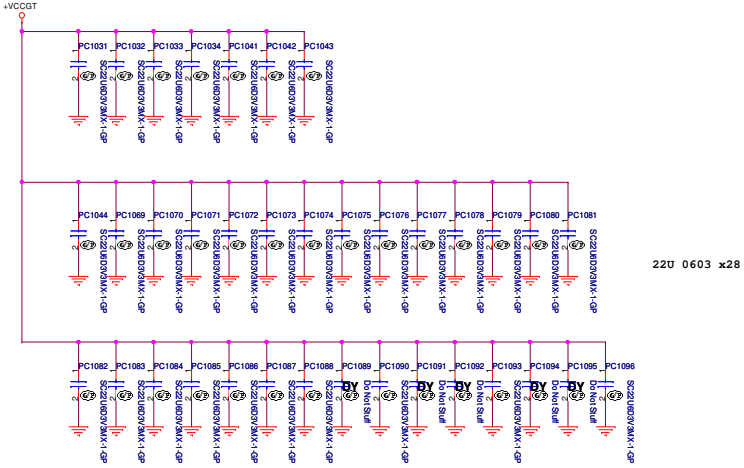


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

Iris SKL UMA

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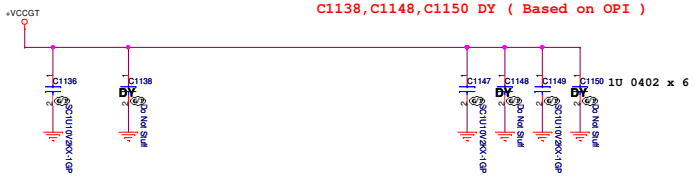
Title: CPU_(Power CAP1)

Size: A2 | Document Number: Iris2 SKL-U | Rev: A00

Date: Tuesday, May 26, 2015 | Sheet 10 of 105

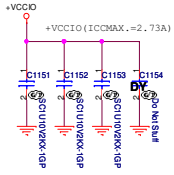
Main Func = CPU

C1138,C1148,C1150 DY (Based on OPI)

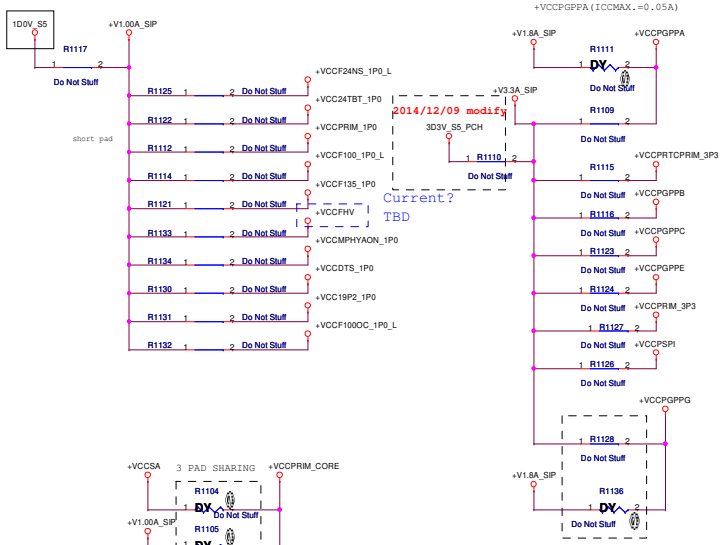


UNSLICED GT

VCCIO



PCH DERIVED RAILS



GTUS

20141114 Alden

+V_VCCGTUS_VR can merge to +VCCGT

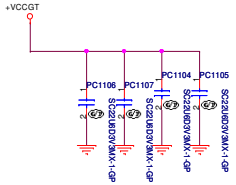
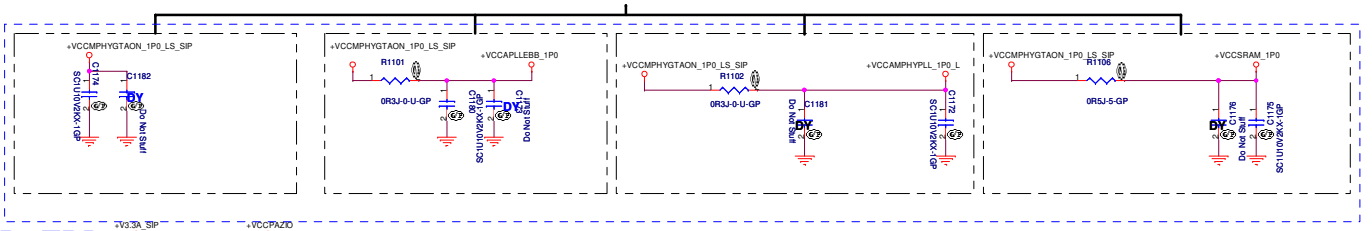
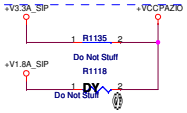


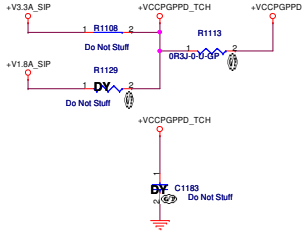
Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

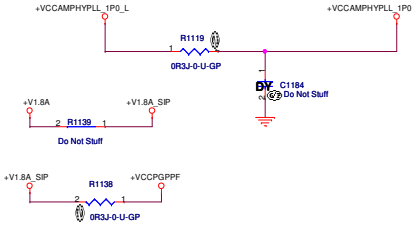
Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		
		(6.3V)[4]	
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible
		5x 22uF 0603	Additional components needed when supporting 23e
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible



CAP TBD







Iris SKL UMA

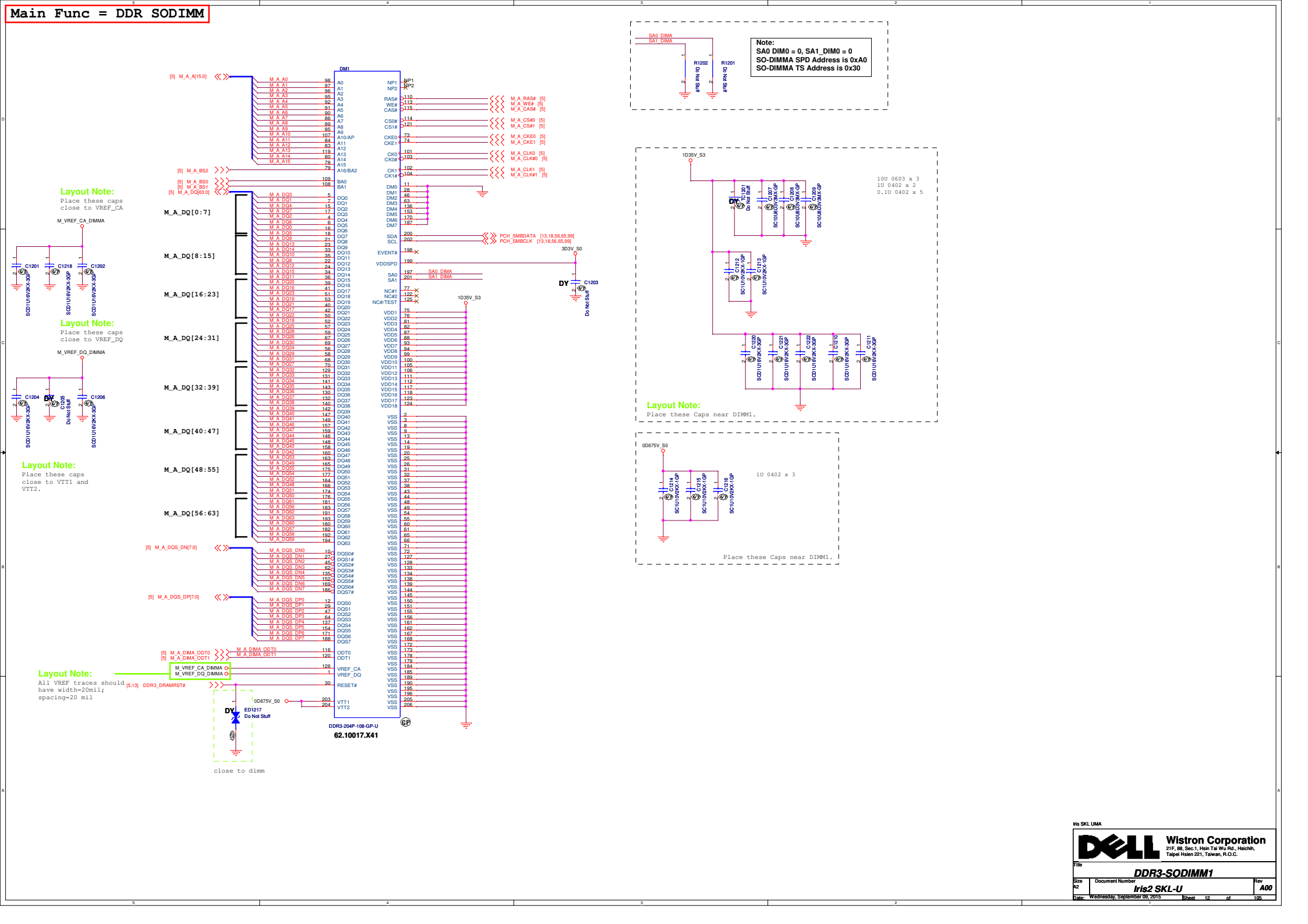
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP2)

Size: A2 | Document Number: Iris2 SKL-U | Rev: A00

Date: Tuesday, May 26, 2015 | Sheet 11 of 105

Main Func = DDR SODIMM



Iris SKL UMA

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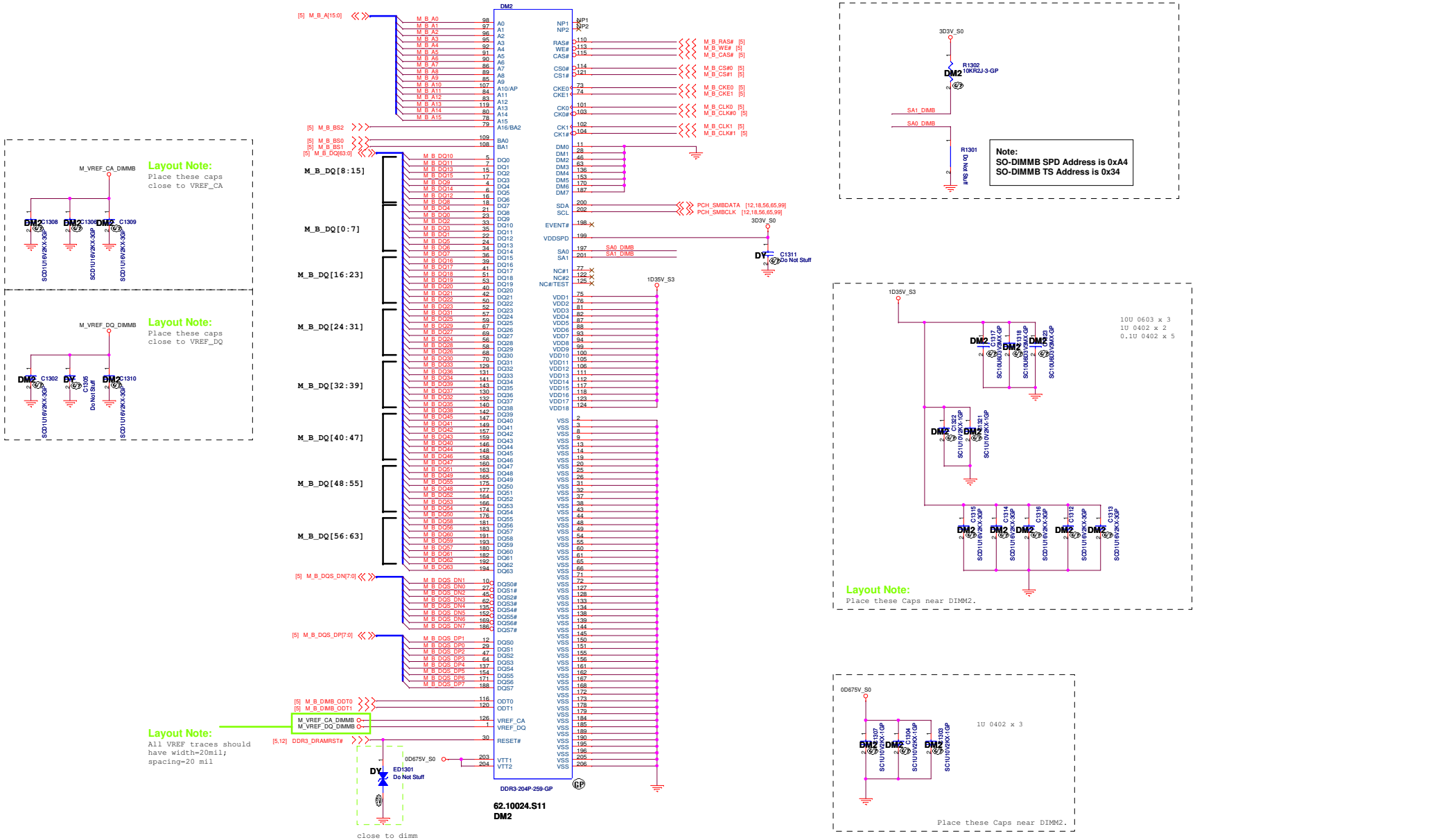
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR3-SODIMM1**

Size	Document Number	Rev
A2	Iris2 SKL-U	A00

Date: Wednesday, September 09, 2015 Sheet 12 of 105

Main Func = DDR SODIMM



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Title	DDR3-SODIMM2	
Size: A2	Document Number: Iris2 SKL-U	Rev: A00
Date: Wednesday, September 09, 2015	Sheet 13 of 105	

(Blanking)

Iris SKL UMA

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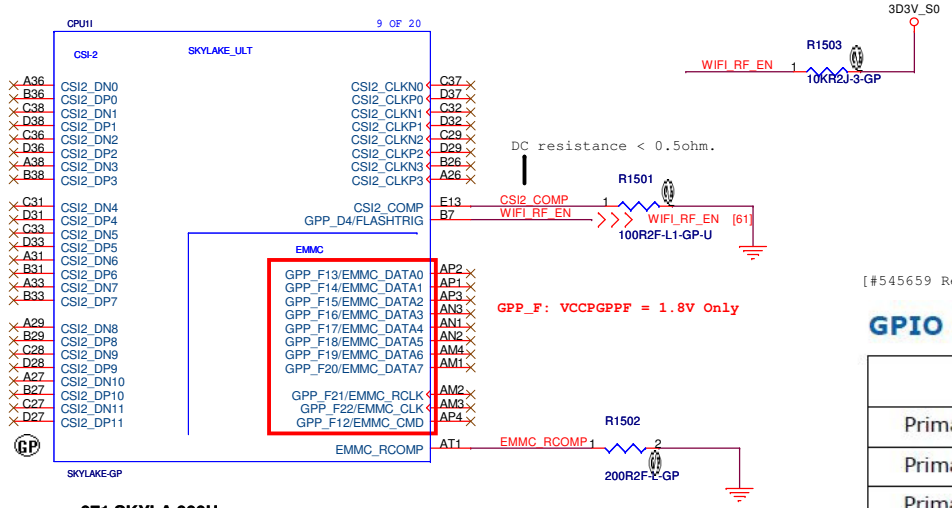
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)_SODIMM _SODIMM4*

Size	Document Number	Rev
A4	*Iris2 SKL-U*	*A00*

Date: Tuesday, May 26, 2015 Sheet 14 of 105

Main Func = PCH



071.SKYLA.000U

Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

Iris SKL UMA

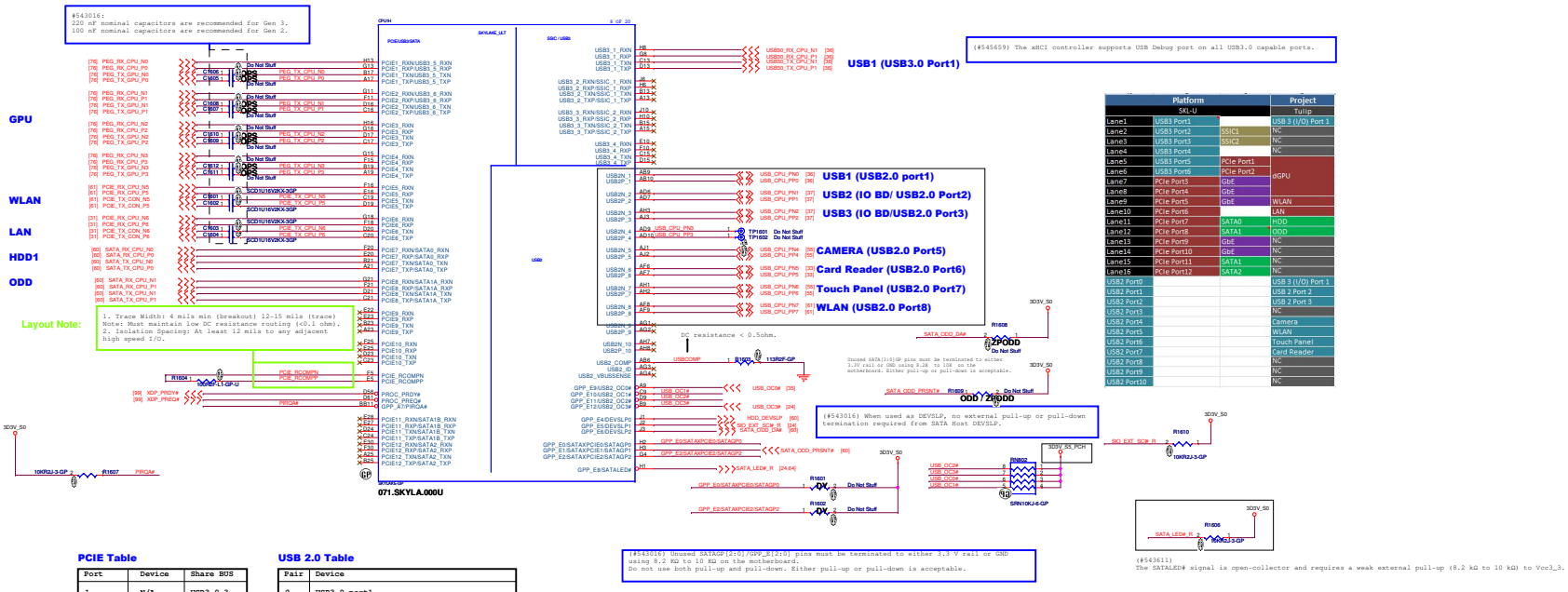
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(CS-2/EMMC)

Size: A3 | Document Number: Iris2 SKL-U | Rev: A00

Date: Wednesday, September 09, 2015 | Sheet 15 of 105

Main Func = PCH



Platform SKL-U	Project Tulip
Lane1 USB3 Port1	USB 3 (I/O) Port 1
Lane2 USB3 Port2 SSIC1	NC
Lane3 USB3 Port3 SSIC2	NC
Lane4 USB3 Port4	NC
Lane5 USB3 Port5 PCIe Port1	dGPU
Lane6 USB3 Port6 PCIe Port2	dGPU
Lane7 PCIe Port3 GbE	dGPU
Lane8 PCIe Port4 GbE	dGPU
Lane9 PCIe Port5 GbE	WLAN
Lane10 PCIe Port6	LAN
Lane11 PCIe Port7 SATA0	HDD
Lane12 PCIe Port8 SATA1	ODD
Lane13 PCIe Port9 GbE	NC
Lane14 PCIe Port10 GbE	NC
Lane15 PCIe Port11 SATA1	NC
Lane16 PCIe Port12 SATA2	NC
USB2 Port0	USB 3 (I/O) Port 1
USB2 Port1	USB 2 Port 2
USB2 Port2	USB 2 Port 3
USB2 Port3	NC
USB2 Port4	Camera
USB2 Port5	WLAN
USB2 Port6	Touch Panel
USB2 Port7	Card Reader
USB2 Port8	NC
USB2 Port9	NC
USB2 Port10	NC

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5 (L0~L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	ODD	SATA1
6 (L0~L1)	N/A	

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB2.0 Port2 (Debug Port/IOBD)
2	USB2.0 Port3 (IOBD)
3	X
4	CAMERA
5	Card Reader
6	Touch Panel
7	WLAN

#545659 (SKL_PCH_U_Y_EDS Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

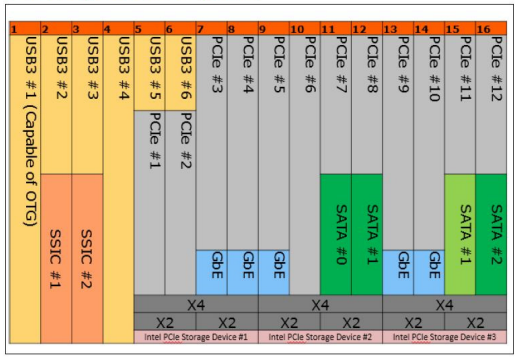


Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

Iris SKL UMA

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Title: CPU (PCIE/SATA/USB)

Size	Document Number	Rev
A1	Iris2 SKL-U	A00

Date: Wednesday, September 09, 2015 Sheet 16 of 155

Main Func = PCH

PCH strap pin: At which pinout for SKL?

On Die DSW VR Enable	
DSWVRMEN	Low = Disable High = Enable (default) *

This signal has no integrated pull-up/pull-down.

Layout note: 3 PAD SHARING

#544669 (CRB): 330k.

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

DY for OBFF disable

[#543016 Rev0.7]
EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k pull-down that is active during the early portion of the power up sequence

BATLOW#:
Pull-up required even if not implemented.

SYSTEM POWER MANAGEMENT
SKYLAKE_ULT
SKYLAKE-GP
071.SKYLA.000U

+VCCMPHYGTAON_1P0

SKL: 1.0V
+VCCMPHYGTAON_1P0 (ICCMAX.=3.5A)

2015/04/20 modify

2015/02/10 modify

Jis-wire with XDP_PM_RSMRST_PWRGD_XDP

Modify on 20150204

DS3 BOM Option

NON DS3

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

VCCST_PWRGD / HWM201:

VCCST_PWRGOOD

- VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

Iris SKL UMA

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Title: CPU_(POWER MANAGEMENT)
Size: A2 | Document Number: Iris2 SKL-U | Rev: A00
Date: Wednesday, September 09, 2015 | Sheet 17 of 105

Main Func = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

SKL MOW 2014WW52 requirement

PLACE WITHIN 1.1 INCH OF PCH

(#543016)Optional, can be left as OPEN/No-Connect.

RCIN#:
Frequency to Avoid: 33 MHz

SERIRQ PH:
PDG: 8.2k
CRB: 10k

Swap on 2014/12/24

GPU
WLAN
LAN

CPU1E
5 OF 20
SPI - FLASH
SPI - TOUCH
C-LINK
SMBUS, SMLINK
LPC
SKYLAKE_ULT
SKYLAKE-GP
071.SKYLA.000U

CPU1U
10 OF 20
CLOCK SIGNALS
SKYLAKE_ULT
SKYLAKE-GP
071.SKYLA.000U

20140820 DAIVD

Iris SKL UMA

Layout: Place at the open door area.

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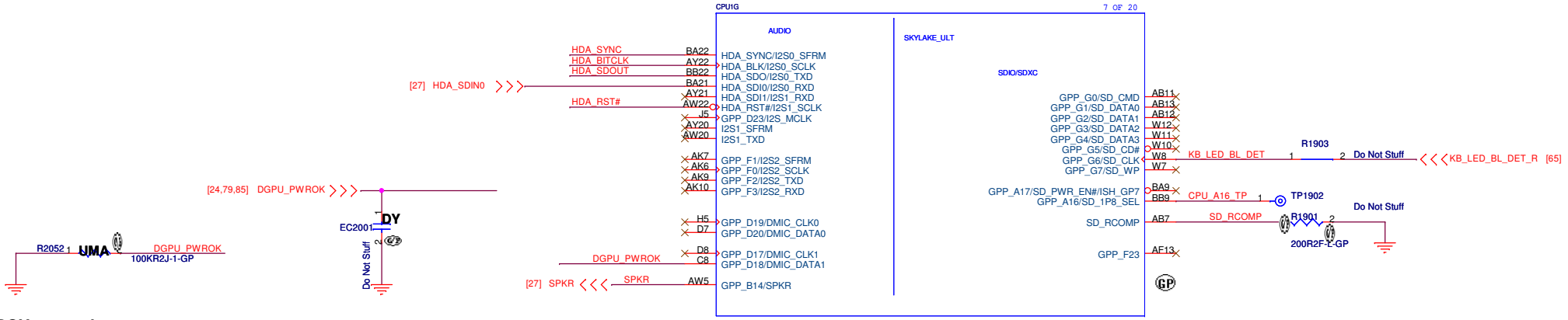
Title: CPU_(LPC/SPI/SMBUS/CL/CLK)

Size	Document Number	Rev
A2	Iris2 SKL-U	A00

Date: Wednesday, September 09, 2015 Sheet 18 of 105

Main Func = PCH



[24,79,85] DGPU_PWROK

R2052 1 UMA DGPU_PWROK 100KR2J-1-GP

EC2001 DY Do Not Stuff

PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default ★ High = Enable

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

NO REBOOT	
HDA_SPKR	★ Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts

3D3V_S0 Do Not Stuff R2006 DY SPKR

[27] HDA_CODEC_BITCLK R1907 33R2J-2-GP HDA_BITCLK

[27] HDA_CODEC_SYNC R1908 Do Not Stuff HDA_SYNC

[27] HDA_CODEC_RST# R1911 Do Not Stuff HDA_RST#

[27] HDA_CODEC_SDOUT R1912 33R2J-2-GP HDA_SDOUT

[24] ME_FWP_EC R1909 1KR2J-1-GP

EC1901 DY Do Not Stuff HDA_CODEC_BITCLK

HDA_CODEC_RST# EC1902 DY Do Not Stuff

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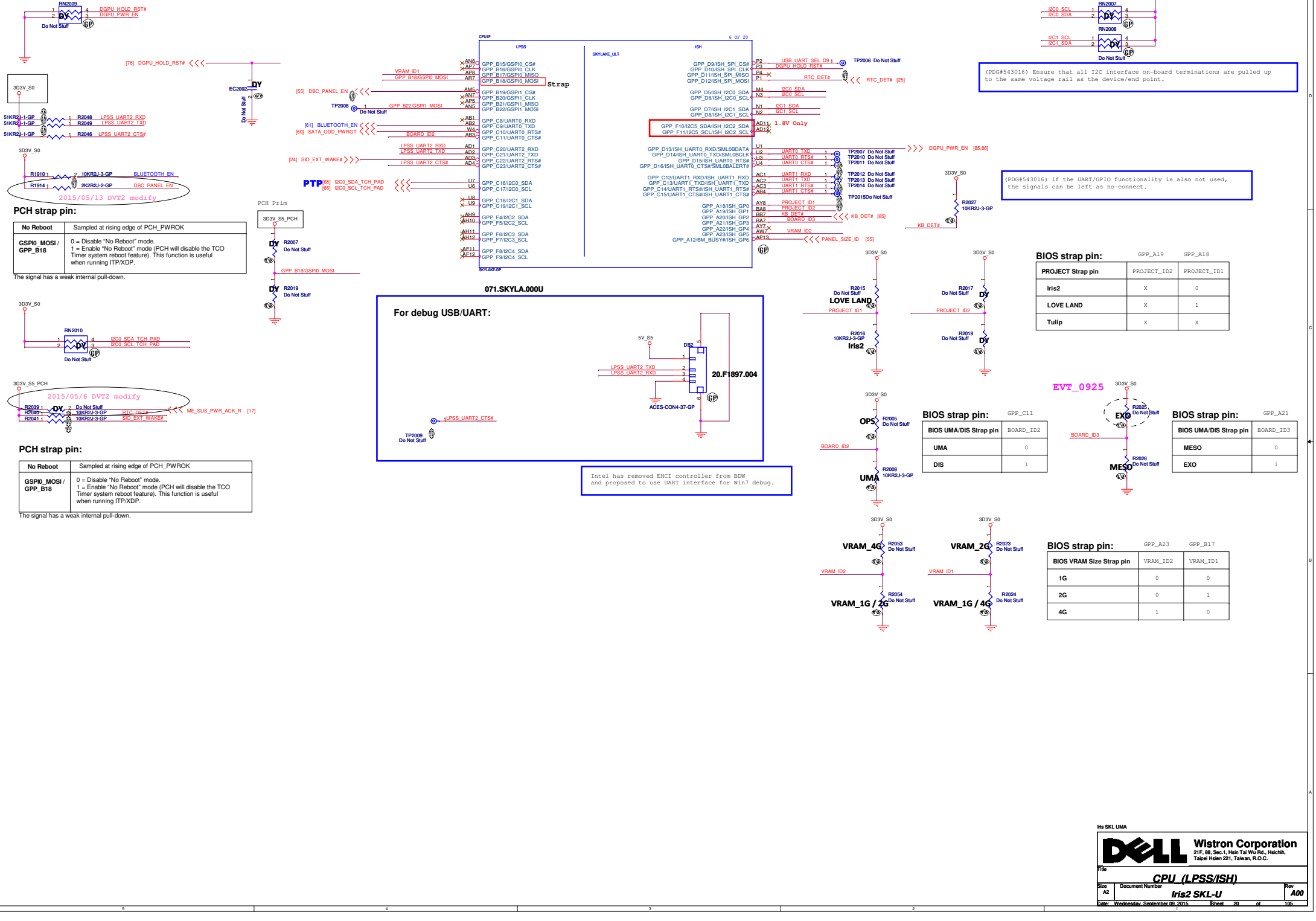
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(AUDIO/SDIO/SDXC)

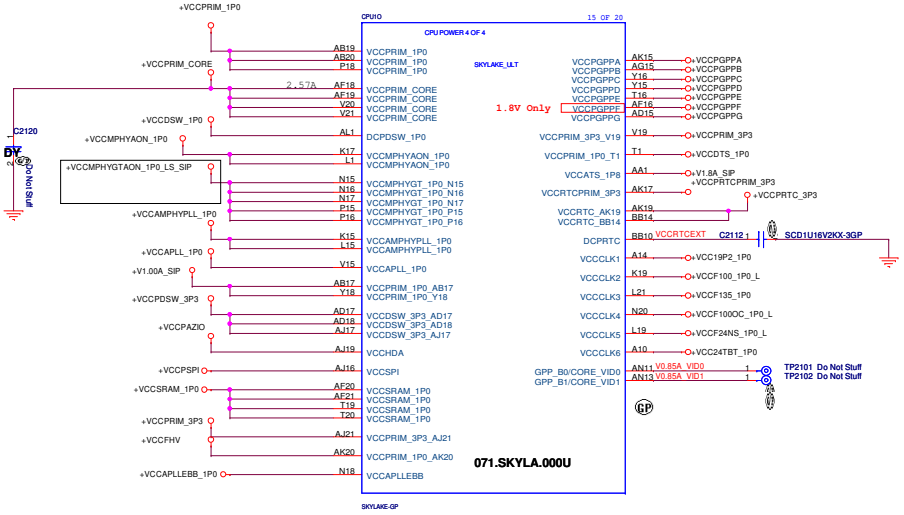
Size	Document Number	Rev
A3	Iris2 SKL-U	A00

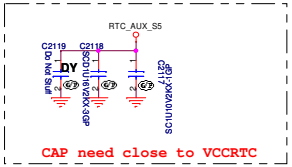
Date: Wednesday, September 09, 2015 Sheet 19 of 105

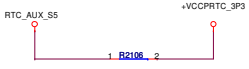
Main Func = PCH

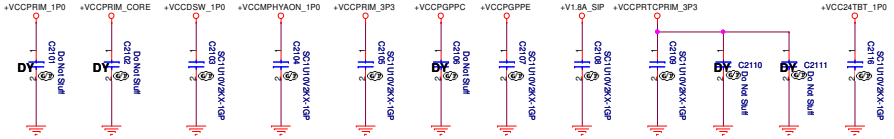


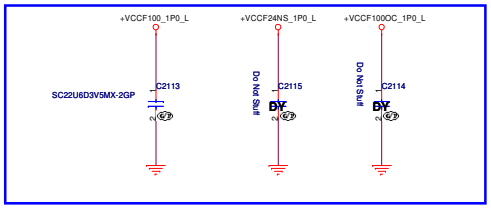
Main Func = PCH











Decoupling and Power Connection Requirements for SKL U PCH (Sheet 1 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V1.0A	VccPRIM	AB19, AB20, P18	1 uF	0402	1	E (<10 mm)	AB19 (Note 1)
	VccMPHYAON	K17, L1	1 uF	0402	1	E (<3 mm)	K17
	VccMPHYGT	N15, N16, N17, P15, P16	1 uF	0402	1	E (<3 mm)	N15
			47 uF	0805	1	E (<10 mm)	N15 (Note 1)
	VccAMPHYPLL	K15, L15	1 uF	0402	1	E (<3 mm)	K15 (Note 1)
	VccAPLL	V15	-	-	-	-	-
	VccPRIM	AB17, Y18	-	-	-	-	-
	VccSRAM	AF20, AF21, T19, T20	1 uF	0402	1	E (<10 mm)	AF20 (Note 1)
	VccAPLLEBB	N18	1 uF	0402	1	E (<3 mm)	N18
	VccPRIM	T1	-	-	-	-	-
	VccCLK1	A14	-	-	-	-	-
	VccCLK2	K19	-	-	-	-	-
	VccCLK3	L21	-	-	-	-	-
	VccCLK4	N20	-	-	-	-	-
	VccCLK5	L19	-	-	-	-	-
	VccCLK6	A10	1 uF	0402	1	E (<3 mm)	A10 (Note 1)
V1.0A / V0.85A	VccPRIM_Core	AF18, AF19, V20, V21	1 uF	0402	1	E (<10 mm)	AF18 (Note 1)
V1.0A / V2.4A	VccPRIM	AK20	-	-	-	-	-
V3.3A	VccPRIM	V19, AJ21	1 uF	0402	1	E (<3 mm)	V19 (Note 1)
	VccRTCPRIM	AK17	1 uF	0402	1	E (<3 mm)	AK17
			0.1 uF	0402	1		
	VccPGPPB	AG15	1 uF	0402	1	E (<3 mm)	AG15 (Note 1)
	VccPGPPC	Y16	1 uF	0402	1	E (<10 mm)	Y16 (Note 1)
	VccPGPPE	T16	1 uF	0402	1	E (<10 mm)	T16 (Note 1)
V3.3A/ V1.5A/ V1.8A	VccHDA	AJ19	1 uF	0402	1	E (<10 mm)	AJ19 (Note 1)
V3.3A/ V1.8A	VccSPI	AJ16	-	-	-	-	-
	VccPGPPA	AK15	-	-	-	-	-
	VccPGPPD	Y15	-	-	-	-	-
	VccPGPPG	AD15	-	-	-	-	-
V3.3DSW (3.3V)	VccDSW	AD17, AD18, AJ17	-	-	-	-	-
V3.3RTC (3.3V)	VccRTC	AK19, BB14	1 uF	0402	1	E (<3 mm)	AK19
			0.1 uF	0402	1		
V1.8A	VccPGPPF	AF16	-	-	-	-	-
	VccATS	AA1	1 uF	0402	1	E (<10 mm)	AA1

Iris SKL UMA

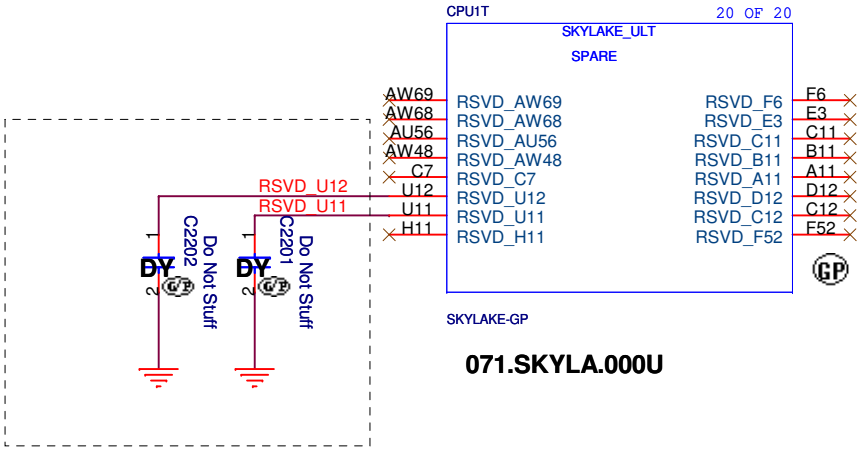
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER1)

Size: A2 | Document Number: Iris2 SKL-U | Rev: A00

Date: Tuesday, May 26, 2015 | Sheet 21 of 105

Main Func = PCH



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SKL MOW 2014WW52 requirement

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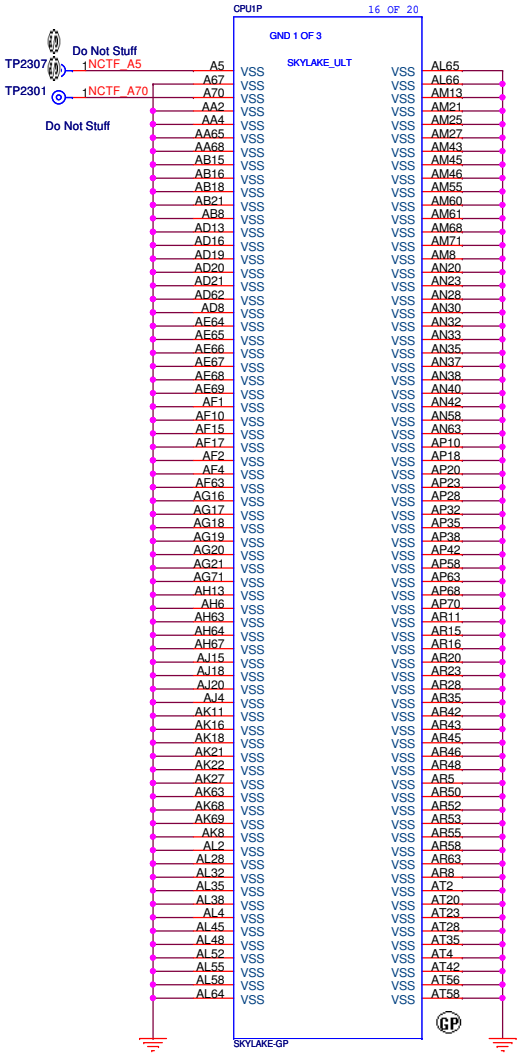
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU_(RSVD)*

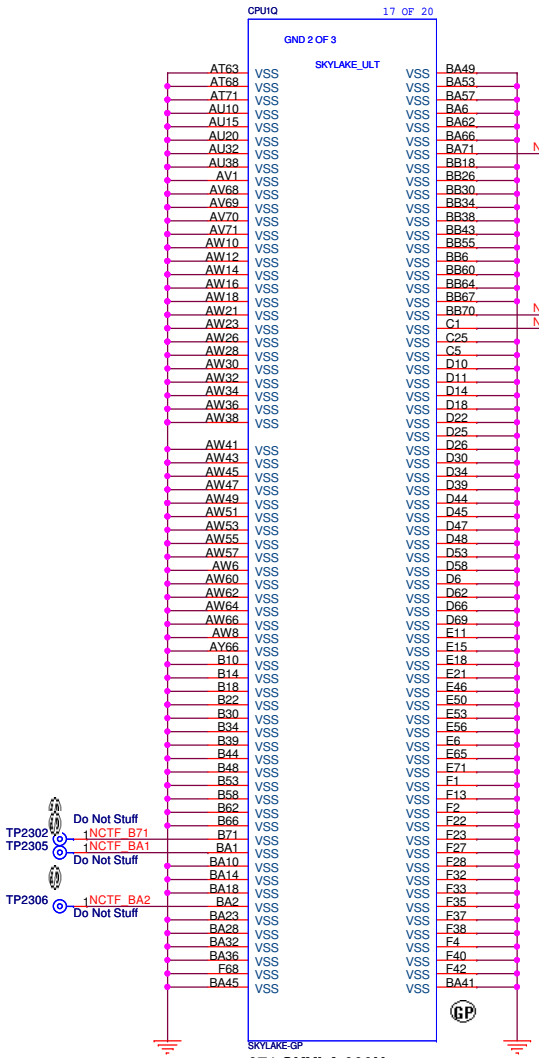
Size	Document Number	Rev
A4	*Iris2 SKL-U*	*A00*

Date: Tuesday, May 26, 2015 Sheet 22 of 105

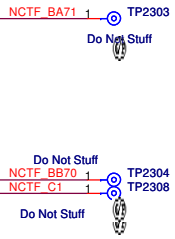
Main Func = PCH

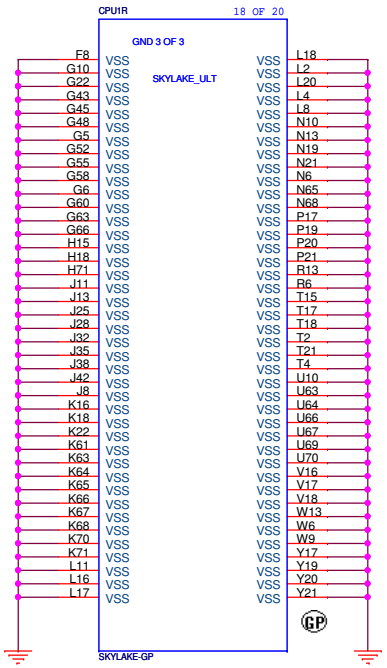


071.SKYLA.000U



071.SKYLA.000U





[#543016 Rev0.9]

071.SKYLA.000U

Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

Iris SKL UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(VSS)

Size: A3 | Document Number: Iris2 SKL-U | Rev: A00

Date: Tuesday, May 26, 2015 | Sheet 23 of 105

Main Func = KBC

20140814 DAVID

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
M00 (SA)	100.0K	10.0K	3.0V
X00 (SB)	100.0K	20.0K	2.75V
X01 (SC)	100.0K	33.0K	2.48V
X02 (SD)	100.0K	47.0K	2.24V
A00 (1)	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO97)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
TBD	100.0K	10.0K/64.180?5.6DU	3.0V
TBD	100.0K	22.1K/64.25125.6DU	2.75V
Iris2 SKL UMA	100.0K	33.4K/64.32475.6DU	2.492V
TBD	100.0K	47.5K/64.39975.6DU	2.261V
Iris2 SKL DIS	100.0K	64.9K/64.64975.6DU	2.001V
Lenv Ioad UMA	100.0K	76.8K/64.75125.6DU	1.790V
Lenv Ioad UMA	100.0K	120K/64.138?5.6DU	1.490V
TBD	100.0K	200K/64.?0875.6DU	1.099V

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

Layout Note:
Need very close to EC

MEC1404

MEC1404-NU-GP

071.01404.000E

082.30003.0131
2rd = 82.30001.C01

2015/1/14 mofidy
83.R2004.G8F

Q2412 and Q2413 merge
2014/12/23 modify
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

eDP backlight Control from PCH

Modify on 2014/12/09

For TS TEMP test

EC_LCD test
EVT1 2014/10/20

EC_GPIO47 High Active

X00_0805

X00_0811
Change pin define

Power Switch Logic(PSL)
EVT1_1021

2015/1/14 mofidy
EVT1 2014/10/21

NON DS3

NON DS3

Iris SKL UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC SMSC 1404

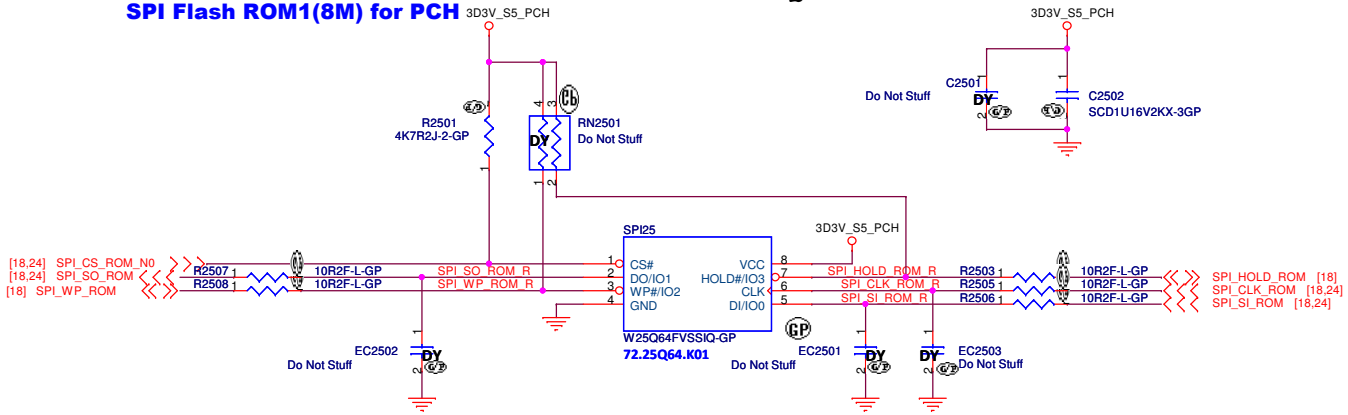
Size	Document Number	Rev
A3	Iris2 SKL-U	A00

Date: Wednesday, September 02, 2015 Sheet 24 of 155

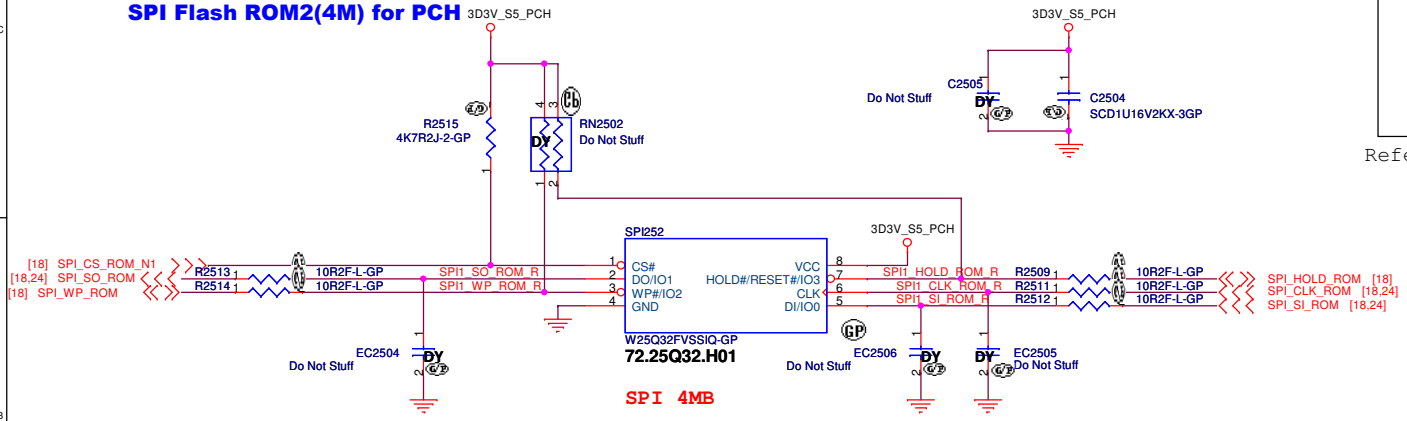
Main Func = SPI Flash

8M:72.25Q64.K01
4M:72.25Q32.H01

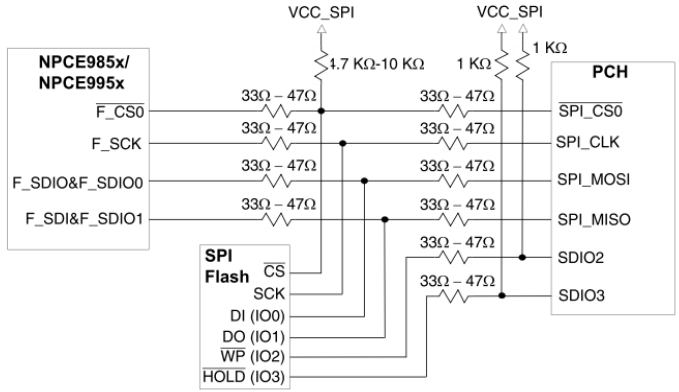
SPI Flash ROM1(8M) for PCH



SPI Flash ROM2(4M) for PCH



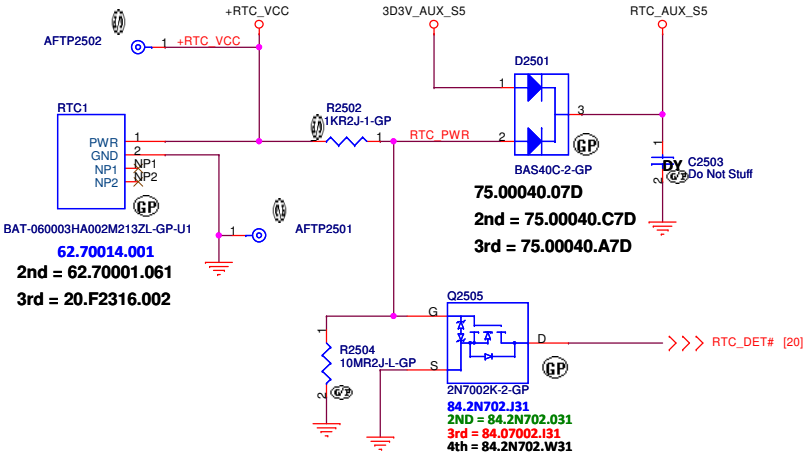
Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.25Q64.K01	O	O	O
72.25647.00A	O	O	O
072.25B64.0001	O	O	O

Main Func = RTC



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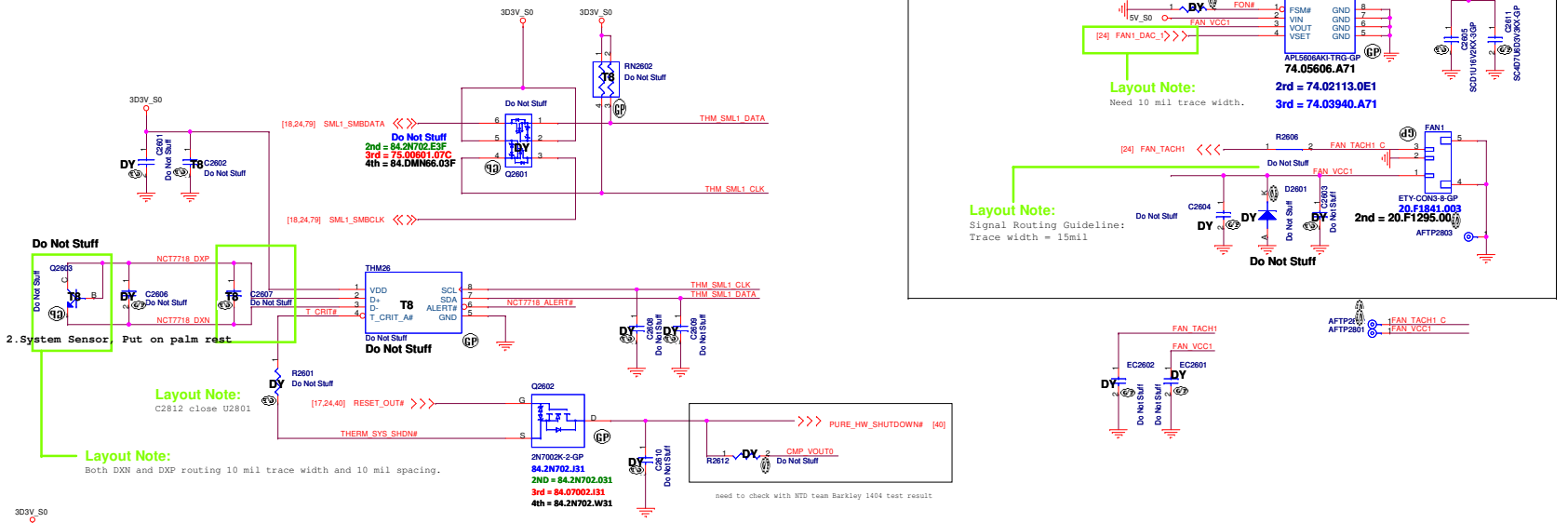
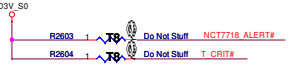
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

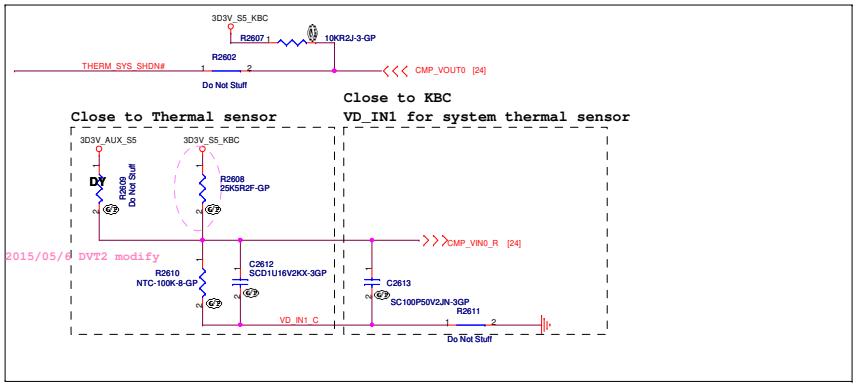
Title: Flash/RTC		
Size: A3	Document Number: Iris2 SKL-U	Rev: A00
Date: Wednesday, September 09, 2015	Sheet 25 of 105	

Main Func = Thermal Sensor

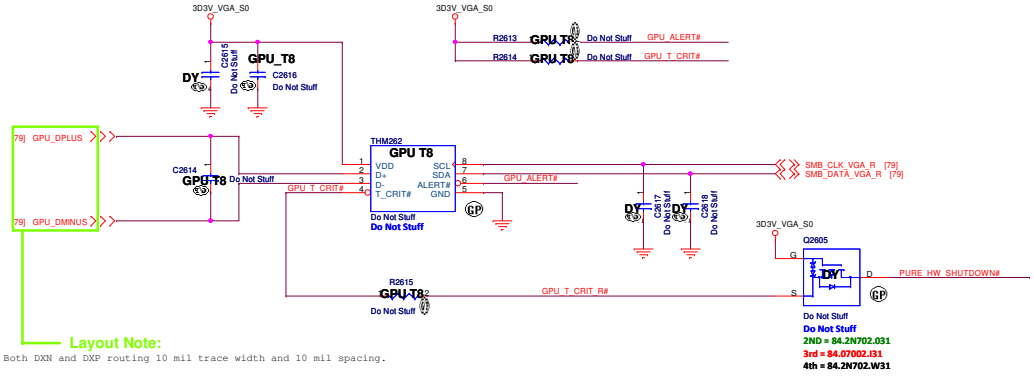




TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



GPU thermal sensor



Iris SKL UMA

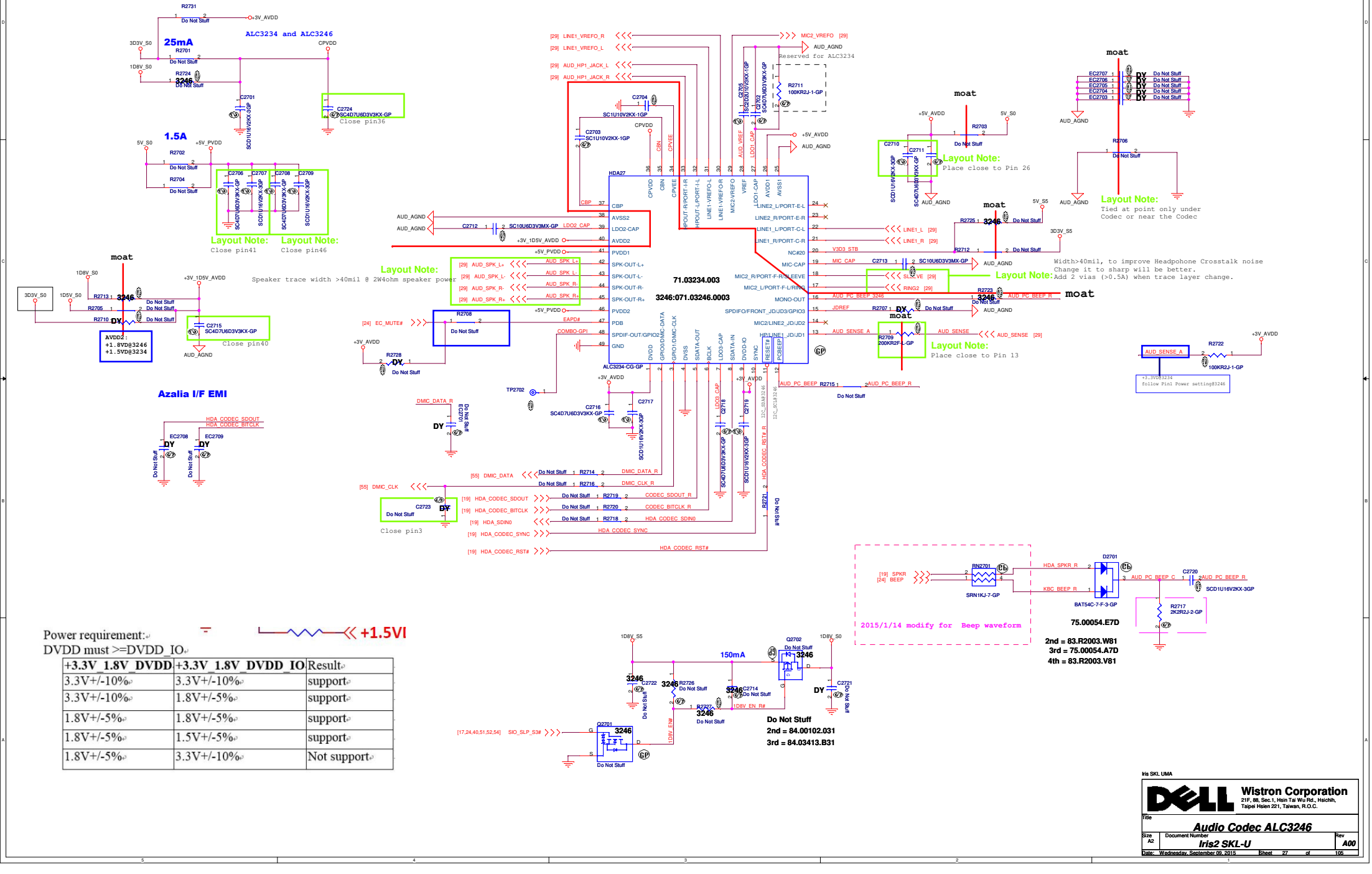
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size: A2 | Document Number: Iris2 SKL-U | Rev: A00

Date: Wednesday, September 09, 2015 | Sheet 26 of 105

Main Func = Audio



Power requirement:

DVDD must >=DVDD_IO

+3.3V_1.8V_DVDD	+3.3V_1.8V_DVDD_IO	Result
3.3V+/-10%	3.3V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	3.3V+/-10%	Not support

Iris SKL UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3246

Size: A2 | Document Number: Iris2 SKL-U | Rev: A00

Date: Wednesday, September 09, 2015 | Sheet 27 of 105

Iris SKL UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

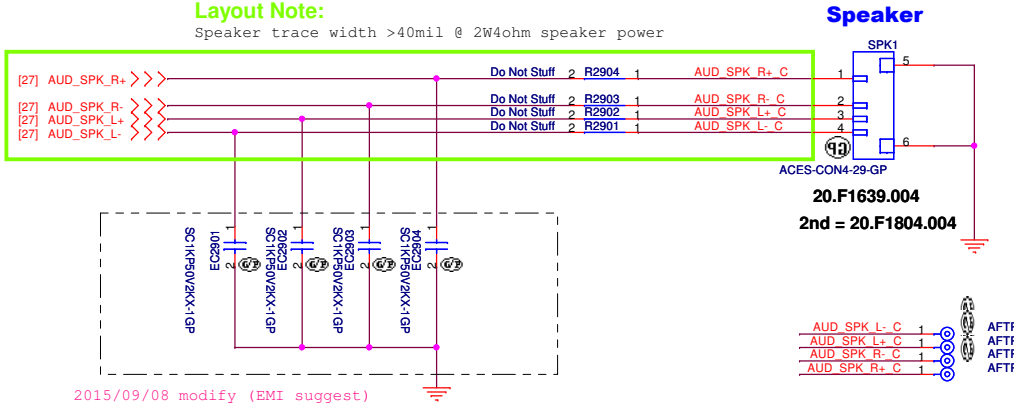
(Reserved)

Size	Document Number	Rev
A1	Iris2 SKL-U	A00

Date: Tuesday, May 26, 2015 Sheet 28 of 155

Main Func = Audio

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

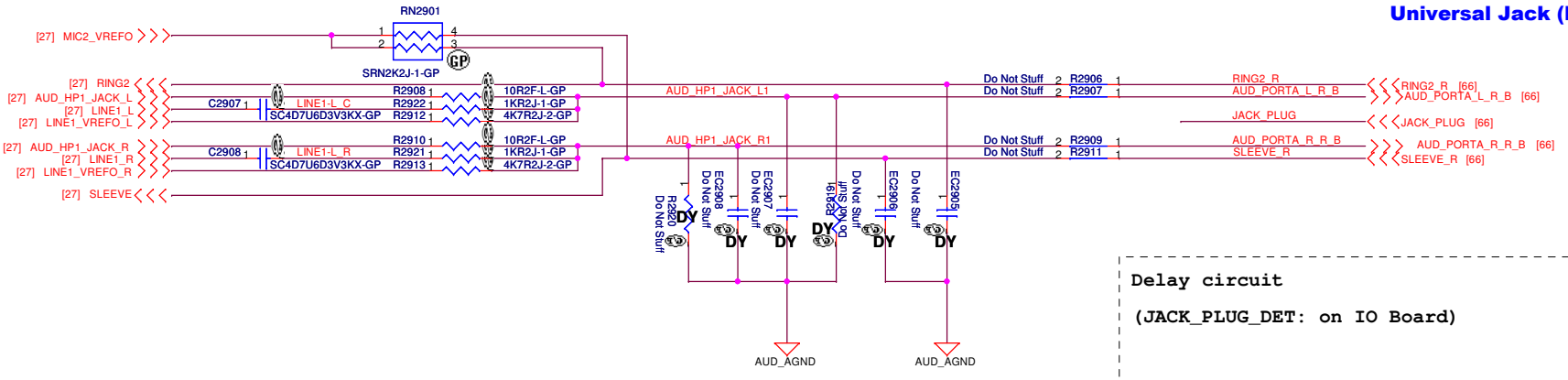


Speaker

20.F1639.004

2nd = 20.F1804.004

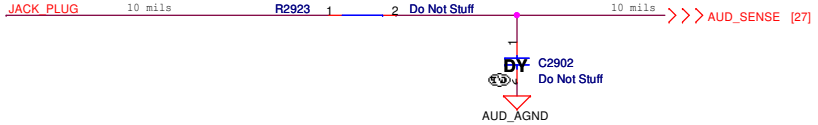
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Universal Jack (Moved to I/O Board)

Delay circuit

(JACK_PLUG_DET: on IO Board)



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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO

Size: A3 | Document Number: Iris2 SKL-U | Rev: A00

Date: Wednesday, September 09, 2015 | Sheet 29 of 105

Main Func = Audio

(Blanking)

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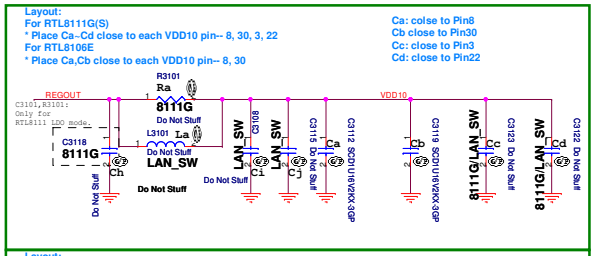
Title
(Reserved)

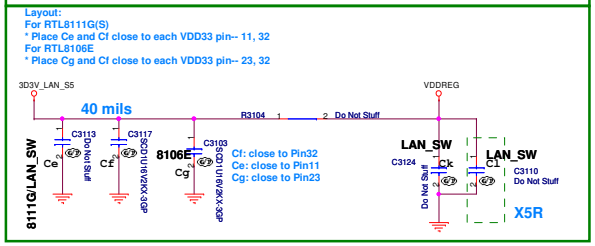
Size	Document Number	Rev
A4	Iris2 SKL-U	A00

Date: Tuesday, May 26, 2015 Sheet 30 of 105

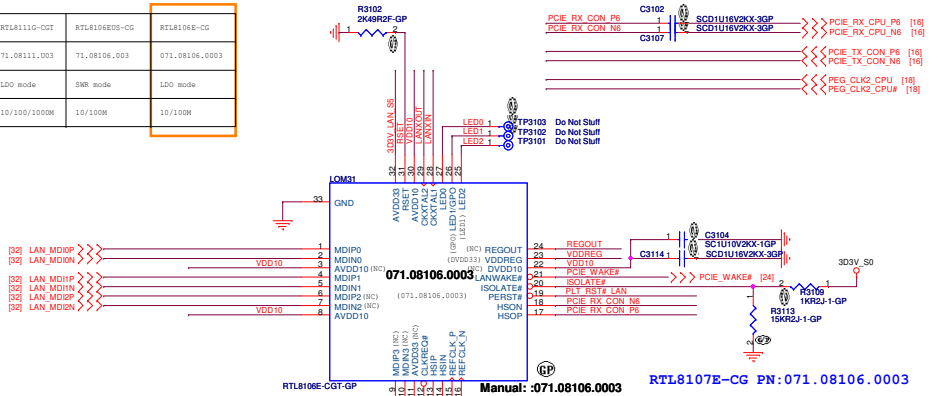
Main Func = LAN

LAN CHIP (10/100/1000M & 10/100M co-lay)





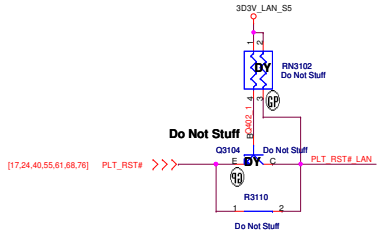
RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CG
71.08111.W03	71.08111.U03	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

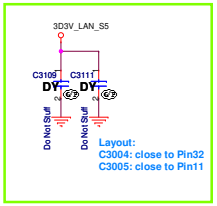


RTL8107E-CG PN:071.08106.0003

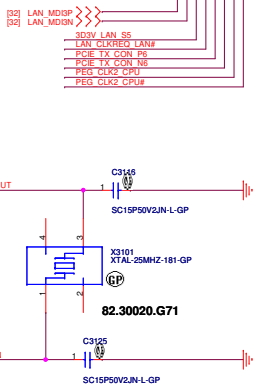
Manual: :071.08106.0003

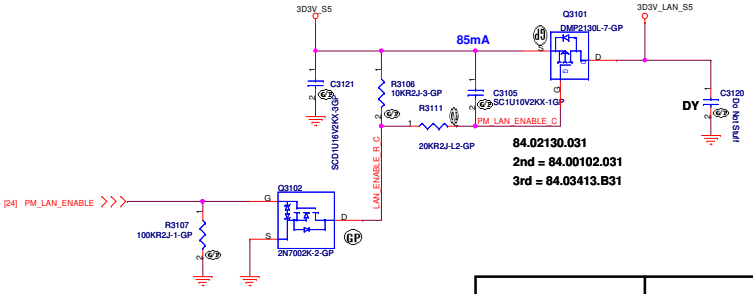
RTL8111G-CGT (71.08111.U03/LDO Mode): 10/100/1000M < 252 mW.
RTL8106E-CG (071.8107E.0A03): 10/100M <70mW.

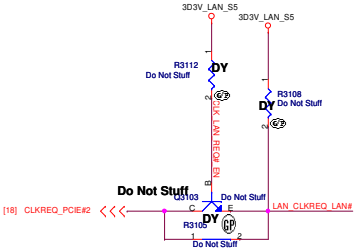




3D3V_LAN_S5 rise time must be controlled between 0.5 mS and 100 mS.







	BOM Option	1.0V Source	Ra	Ch	Cc	Cd	Ce	La	Ci	Cj	Ck	Cl	Cg
RTL8111G-CGT (71.08111.U03)	8111G	LDO	O	O	O	O	O	X	X	X	X	X	X
RTL8111GUS-CG (71.08111.W03)/ RTL8106EUS-CG (71.08106.003)	LAN_SW	SWR	X	X	O	O	O	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	8106E	LDO	X	X	X	X	X	X	X	X	X	X	O

Iris SKL UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

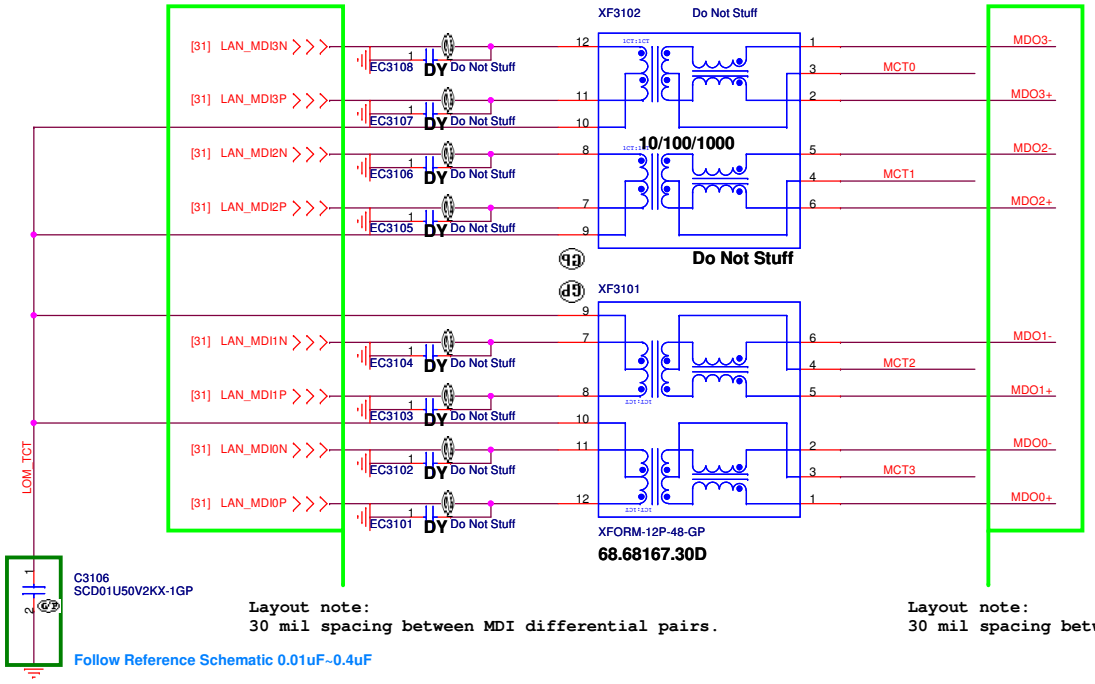
Title: LAN RTL8106

Size: A2 | Document Number: Iris2 SKL-U | Rev: A00

Date: Wednesday, September 09, 2015 | Sheet 31 of 105

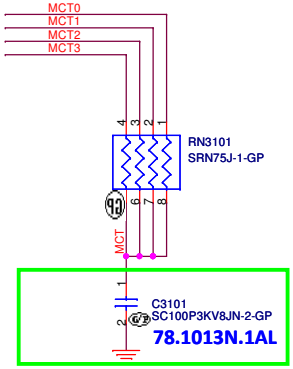
Main Func = LAN

LAN TransFormer (10/100/1000M & 10/100M co-lay)

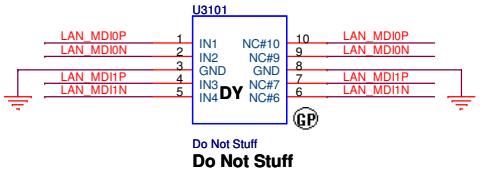


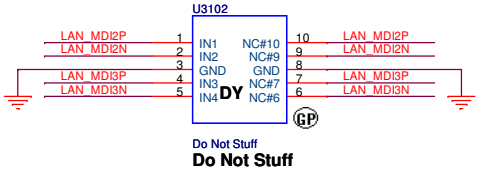
Follow Reference Schematic 0.01uF~0.4uF

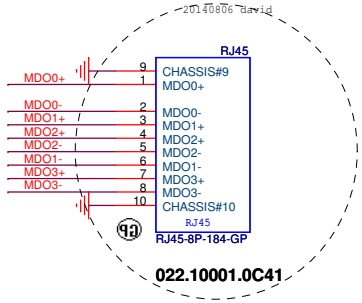
Layout note:
30 mil spacing between MDI differential pairs.



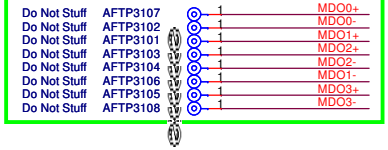
Layout note:
30 mil spacing between MDI differential pairs.







Layout:
Place near RJ45



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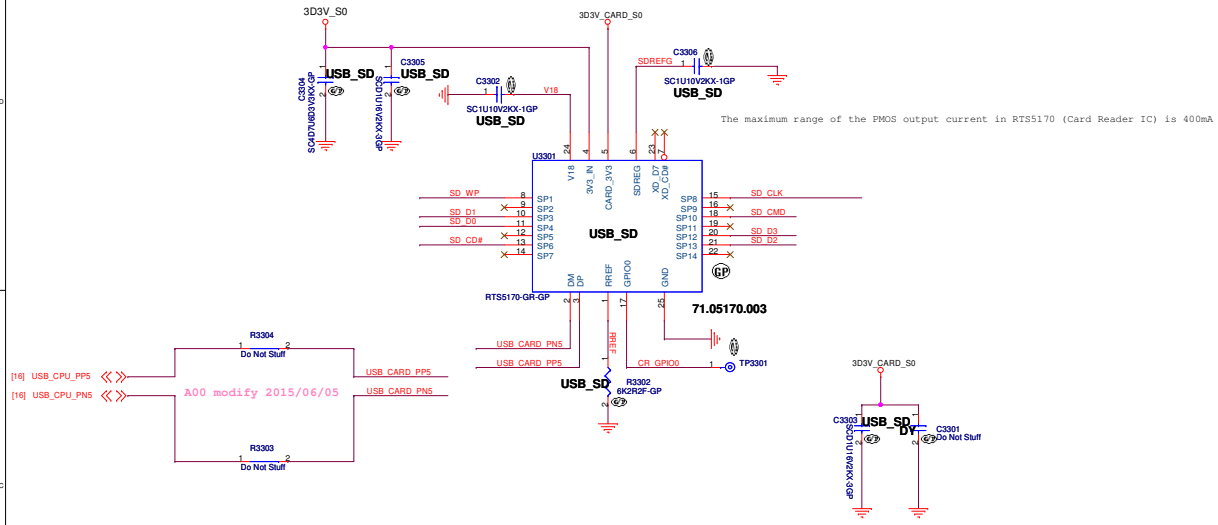
Taipei Hsien 221, Taiwan, R.O.C.

Title	XFOM&RJ45	
Size: A3	Document Number: Iris2 SKL-U	Rev: A00
Date: Wednesday, September 09, 2015	Sheet 32 of 105	

Main Func = Card Reader

Card Reader IC (USB 2.0)

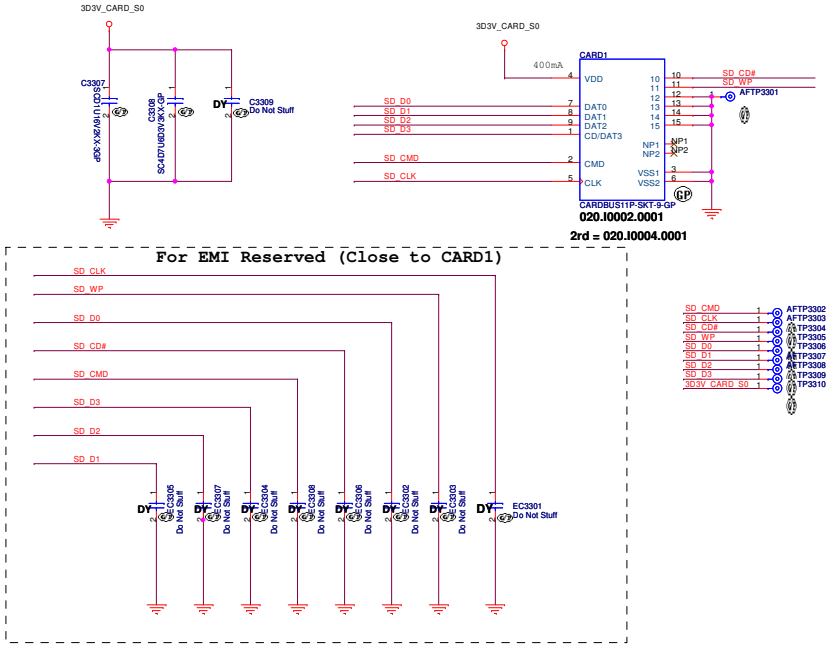


Card Reader Power SW (CPU Only)

Remove 2014/12/23

Co-lay from CPU and Card Reader IC

Remove 2014/12/23



Iris SKL UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Card Reader-RTS5170		
Size: A2	Document Number: Iris2 SKL-U	Rev: A00
Date: Wednesday, September 09, 2015	Sheet 33 of 105	

Main Func = USB3.0 Port1

(Blanking)

Iris SKL UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

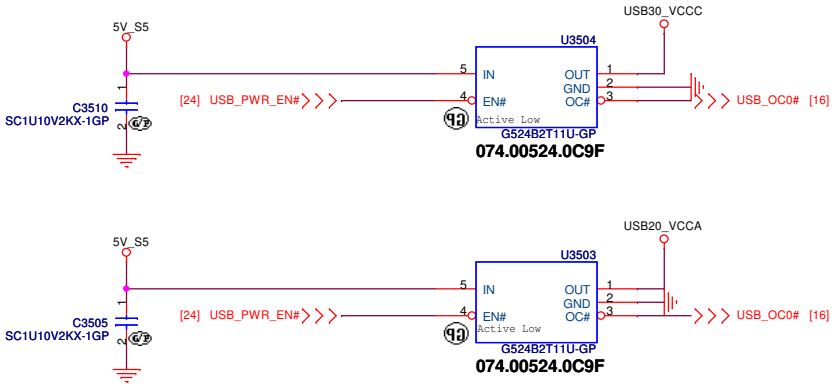
Title

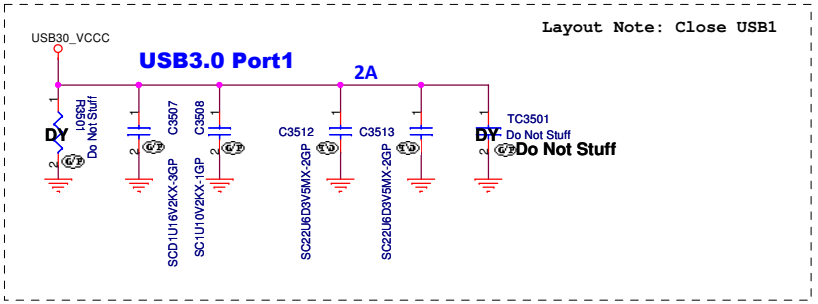
(Reserved)

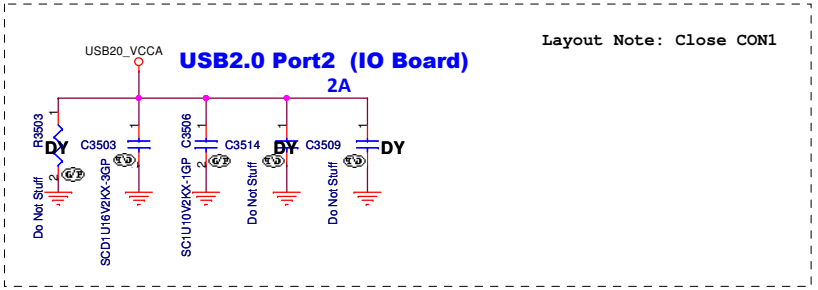
Size	Document Number	Rev
A4	*Iris2 SKL-U*	*A00*

Date: Tuesday, May 26, 2015 Sheet 34 of 105

Main Func = USB3.0 Port1
Main Func = USB2.0 Port2
Main Func = USB2.0 Port3







Iris SKL UMA

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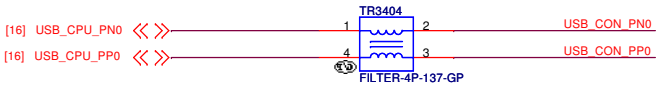
Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB switch		
Size	Document Number: Iris2 SKL-U	Rev: A00
Date: Wednesday, September 09, 2015	Sheet 35 of 105	

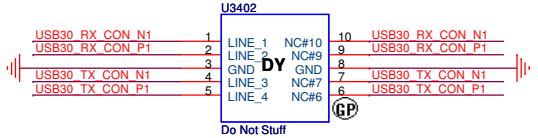
Main Func = USB3.0 Port1

USB2.0 Port2 and USB2.0 Port3 are on IOBD



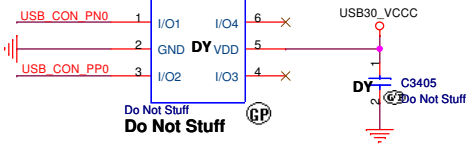
68.01012.20B

A00 modify 2015/06/05



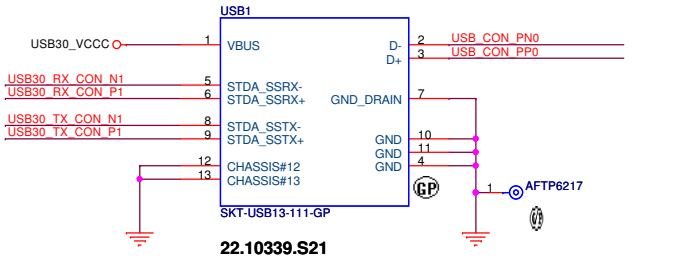
Do Not Stuff

2nd = 75.00107.073

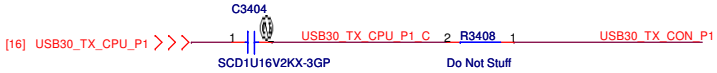


Do Not Stuff

USB3.0 Port1

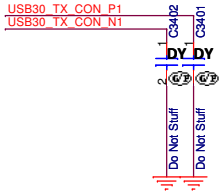


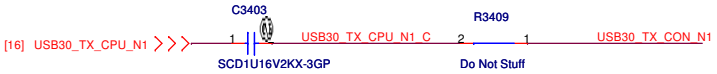
22.10339.S21



A00 modify 2015/06/05

A00 modify 2015/06/05





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Title		
USB30		
Size: A3	Document Number: Iris2 SKL-U	Rev: A00
Date: Wednesday, September 09, 2015	Sheet 36 of 105	

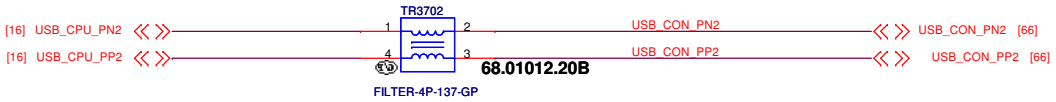
Main Func = USB2.0

USB2 (USB2.0) CMC

A00 modify 2015/06/05

Layout Note:
Close to CON1

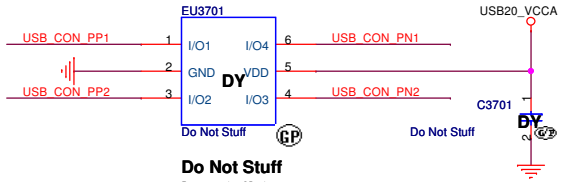
USB3 (USB2.0) CMC



A00 modify 2015/06/05

Layout Note:
Close to CON1

USB ESD Diode



Do Not Stuff

Layout Note:
Close to CON1

Iris SKL UMA

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Title: USB20		
Size: A3	Document Number: Iris2 SKL-U	Rev: A00
Date: Wednesday, September 09, 2015	Sheet 37 of 105	

Main Func = USB3.0 Port1

(Blanking)

Iris SKL UMA

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Title: (Reserved)

Size: A4 | Document Number: Iris2 SKL-U | Rev: A00

Date: Tuesday, May 26, 2015 | Sheet 38 of 105

Main Func = USB3.0 Port1

(Blanking)

Iris SKL UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	*Iris2 SKL-U*	*A00*

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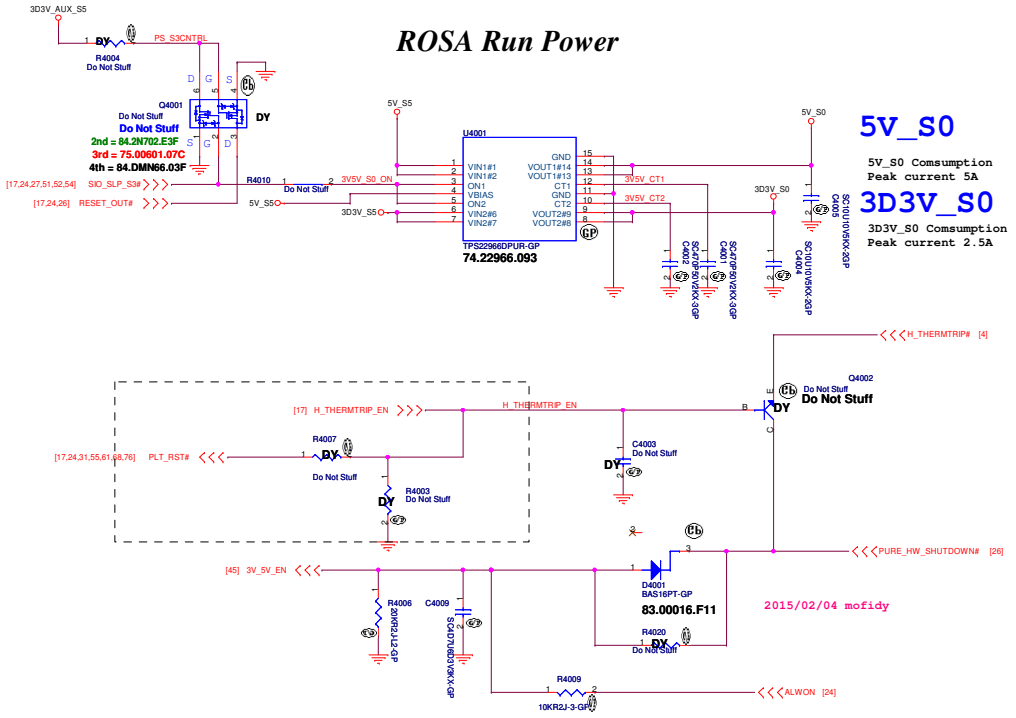
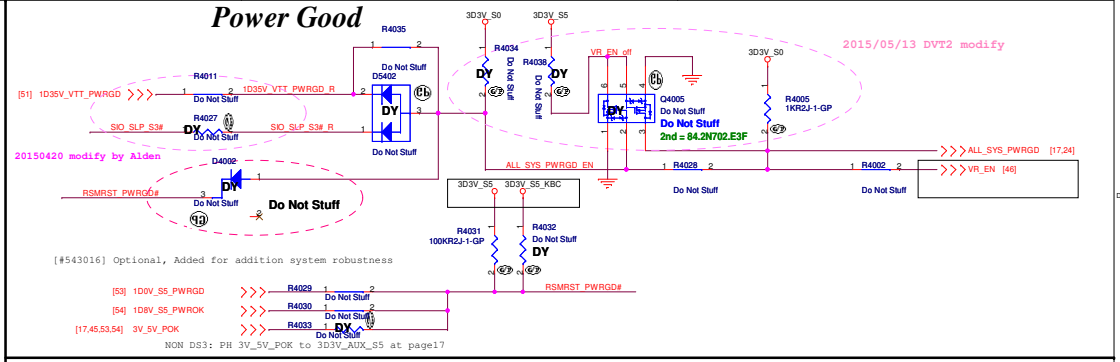
Main Func = Power Plane & Sequence

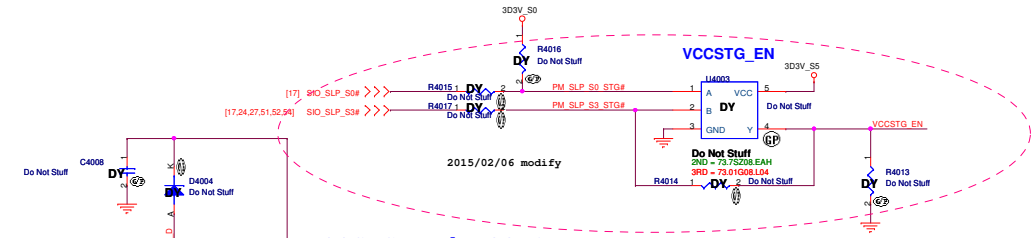
ROSA Run Power



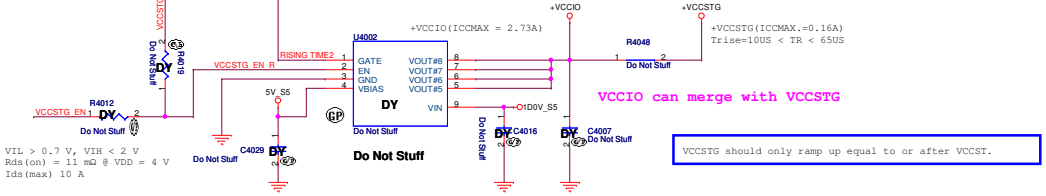
Power Good



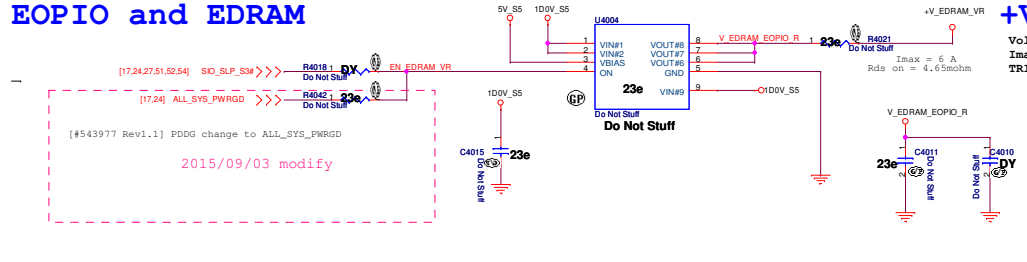
VCCSTG_EN



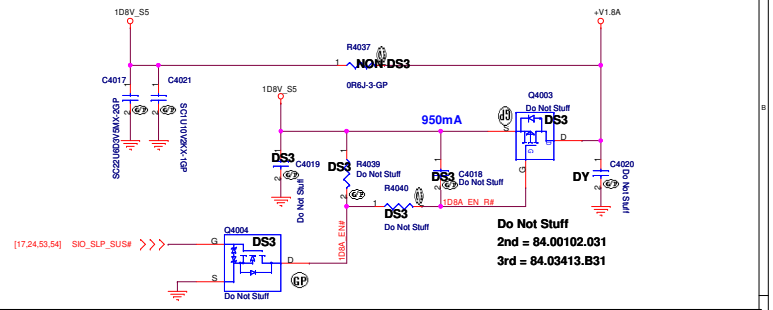
VCCSTG and VCCIO



EOPIO and EDRAM



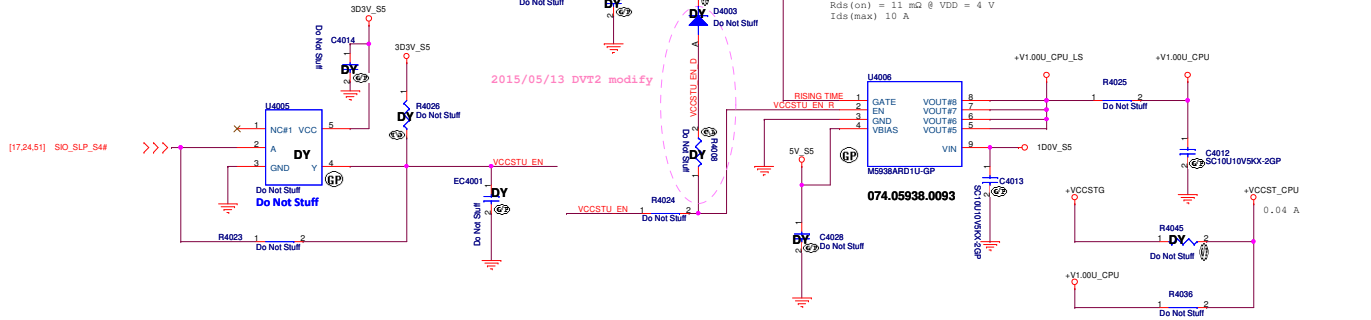
V1.8A



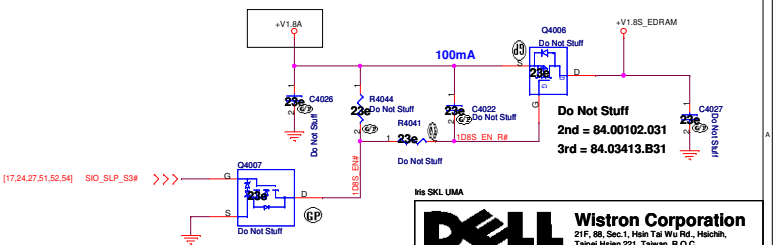
MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

VCCST



V1.8S



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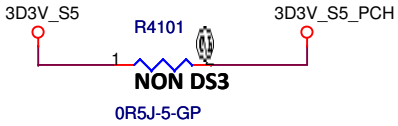
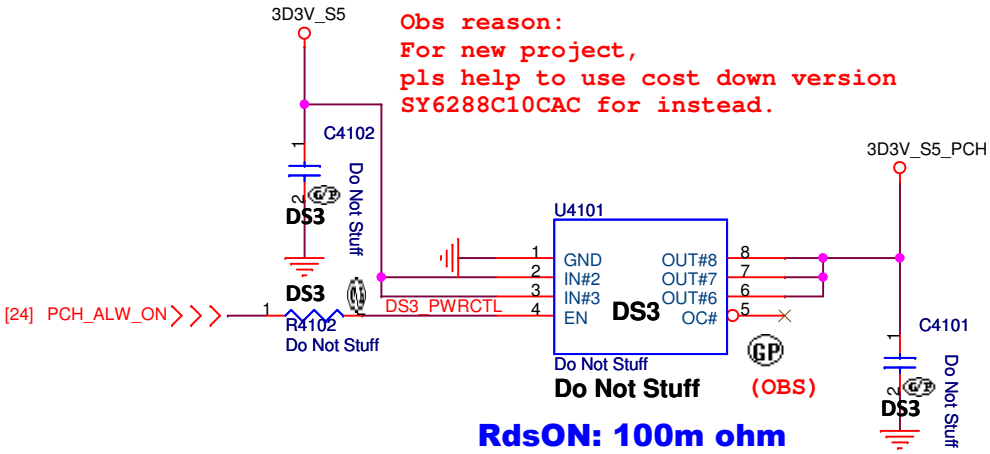
Title: Power Plane Enable

Size	Document Number	Rev
A2	Iris2 SKL-U	A00

Date: Wednesday, September 09, 2015 Sheet 40 of 105

Main Func = Power Plane & Sequence





DS3

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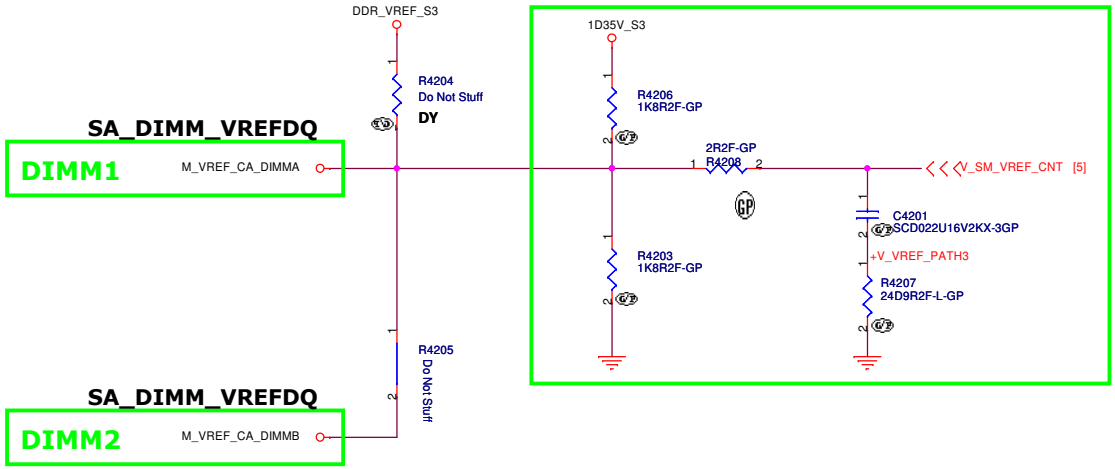
Title	*Connected_Standby(1/2)+DS3*	
Size: A4	Document Number: *Iris2 SKL-U*	Rev: *A00*
Date: Wednesday, September 09, 2015	Sheet 41 of 105	

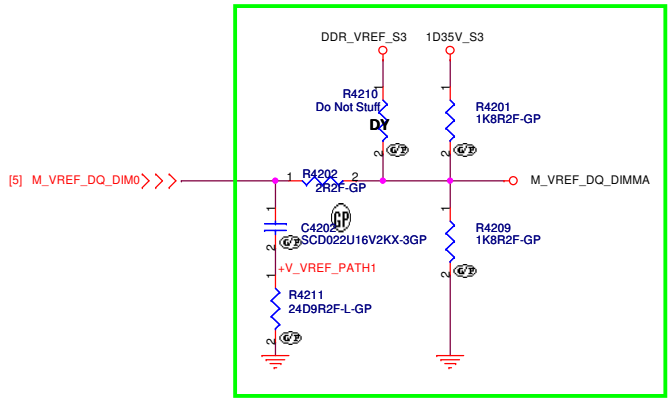
Main Func = DIMM1
Main Func = DIMM2

VREF CIRCUITRY

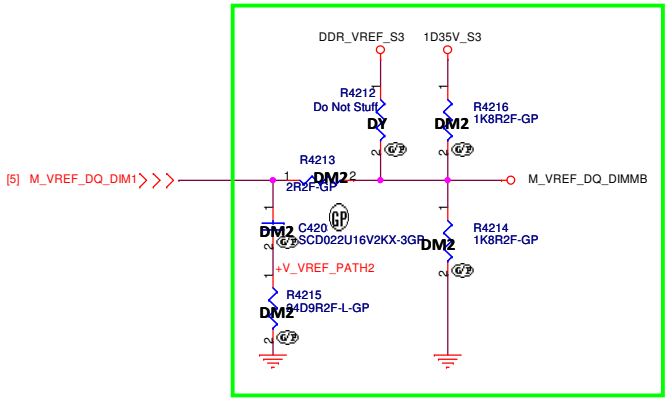
Layout Note:
Place Close DIMMs



Layout Note:
Place Close DIMM1



Layout Note:
Place Close DIMM2



Iris SKL UMA

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Title: Connected_Standby(2/2)

Size: A3 | Document Number: Iris2 SKL-U | Rev: A00

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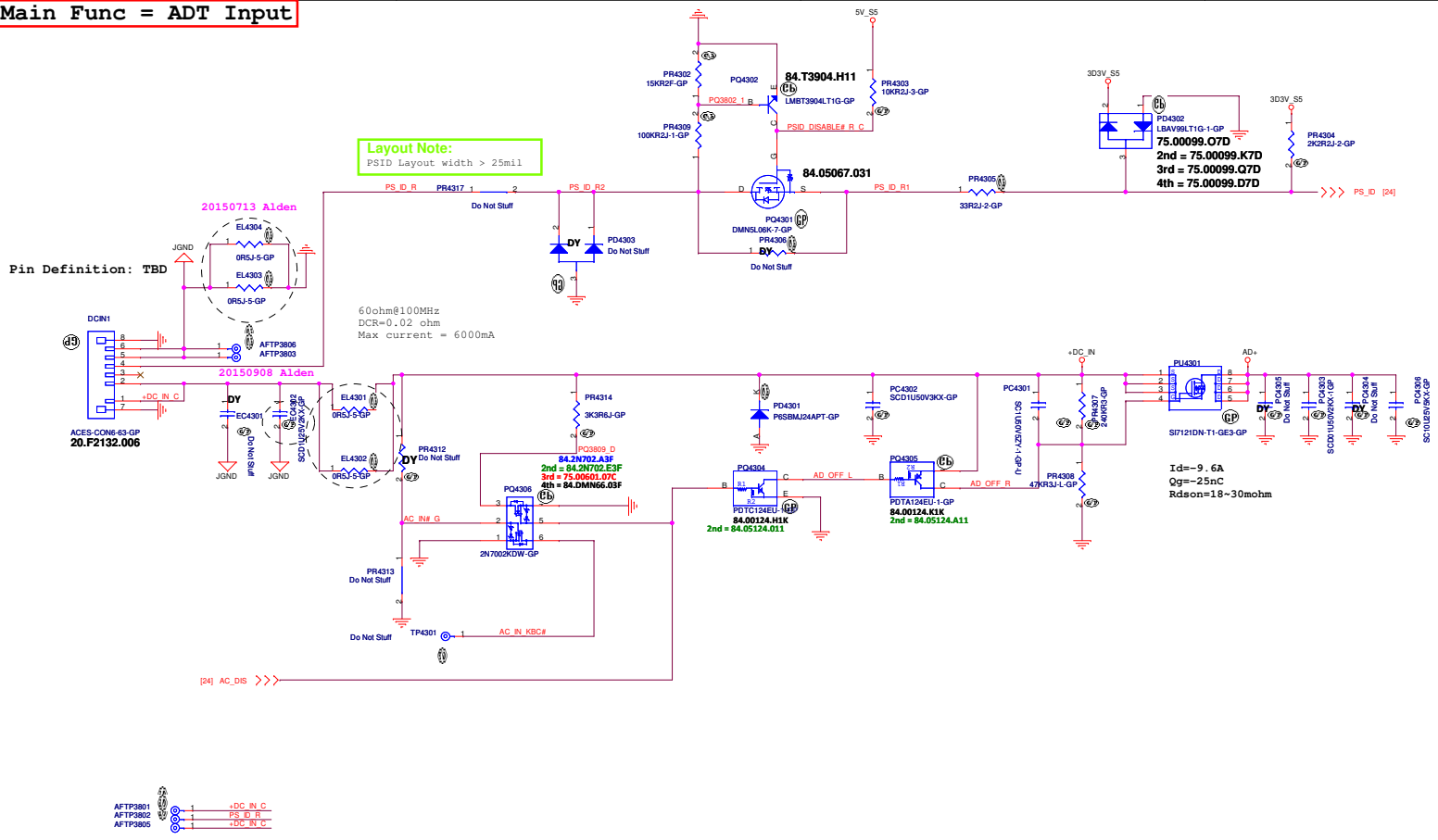
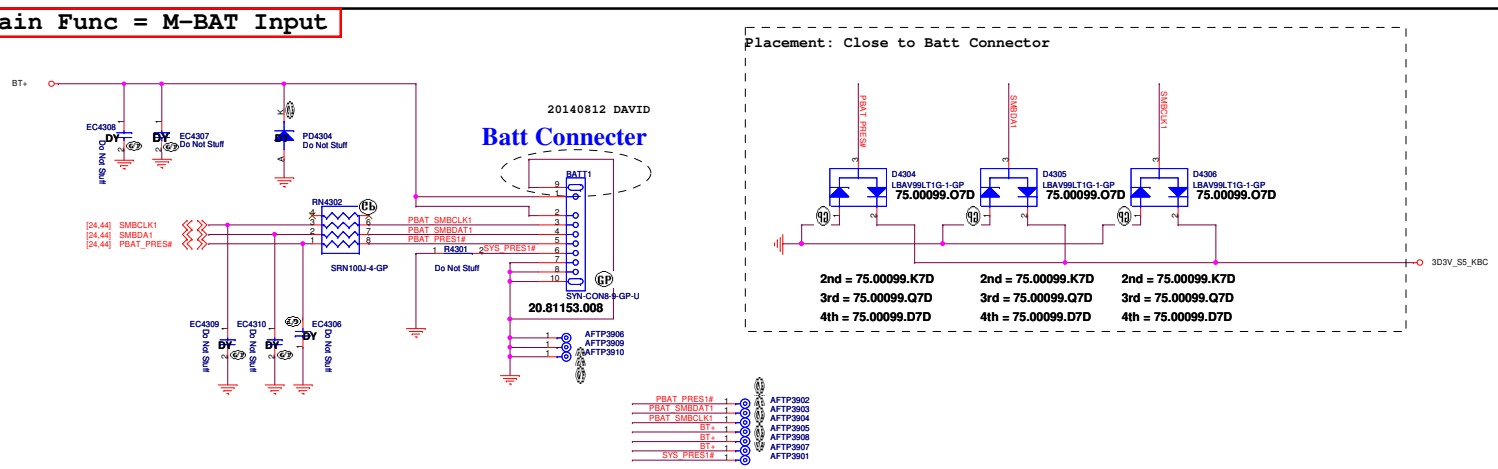
Main Func = ADT Input



Main Func = M-BAT Input



Iris SKL UMA

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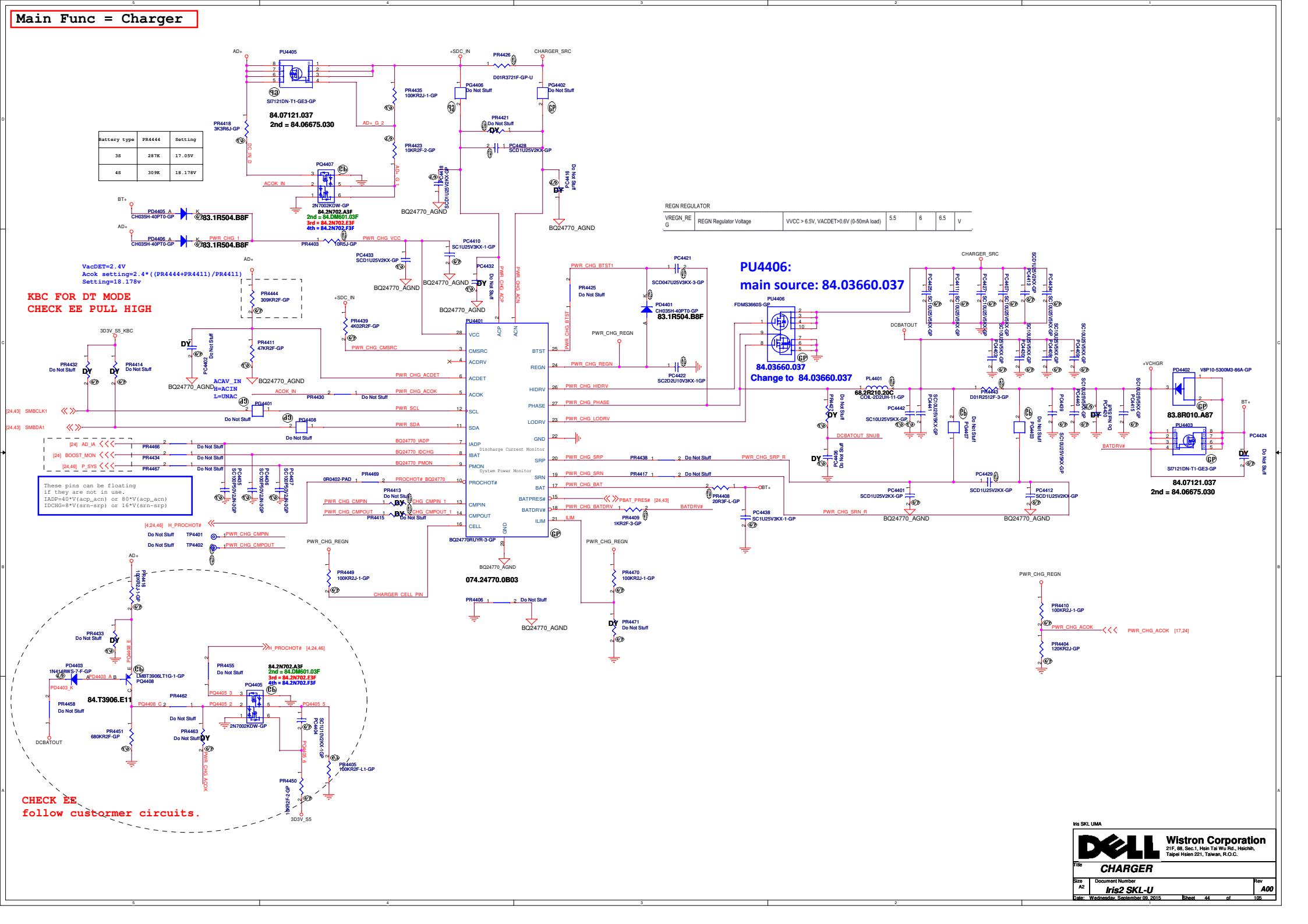
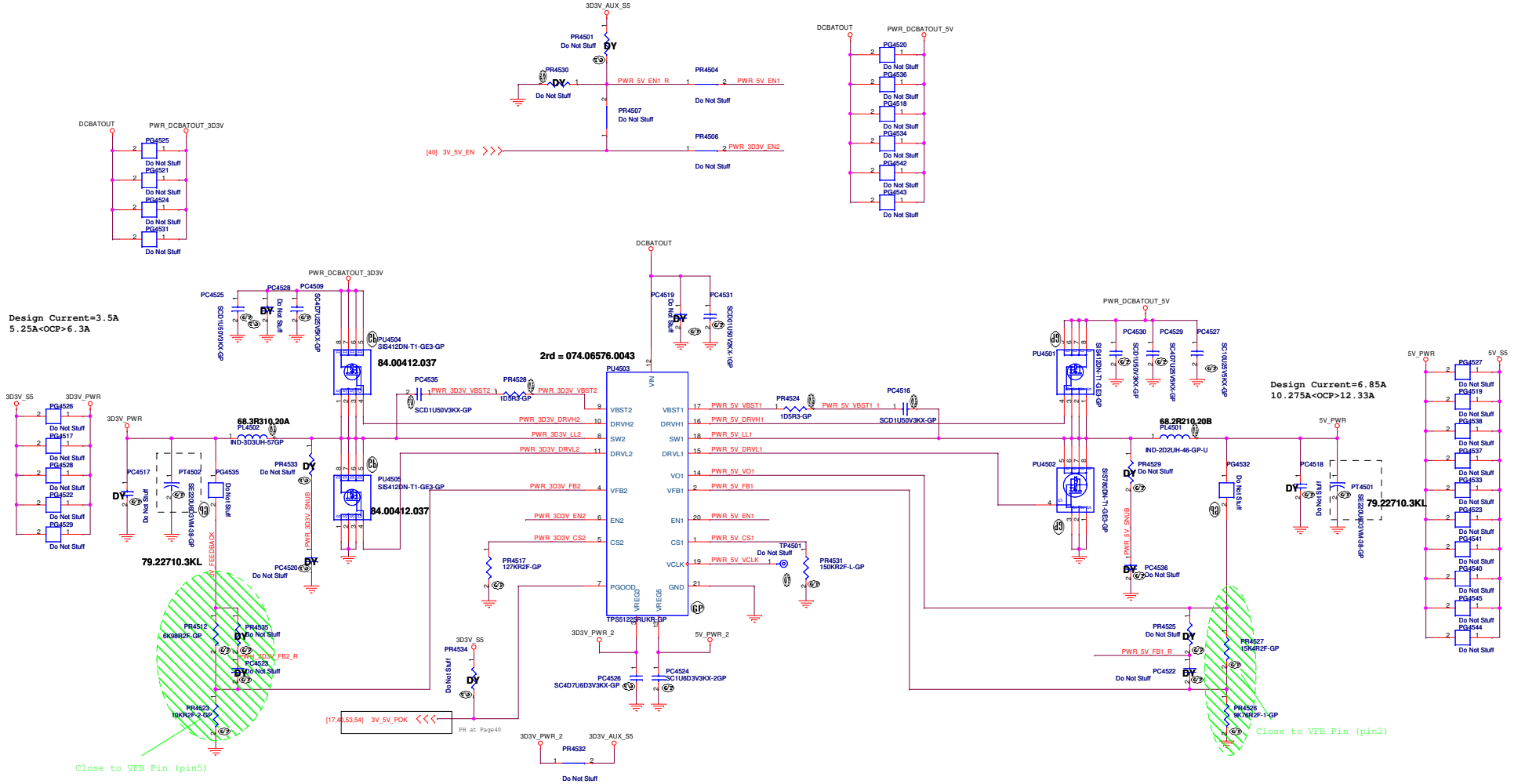
Title		
DCIN		
Size: A2	Document Number: Iris2 SKL-U	Rev: X02
Date: Wednesday, September 09, 2015	Sheet 43 of 105	

Main Func = Charger



Main Func = 3D3V_5V



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

Iris SKL UMA

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Title: DCDC-3D3V&5V

Size	Document Number	Rev
A2	Iris2 SKL-U	A00

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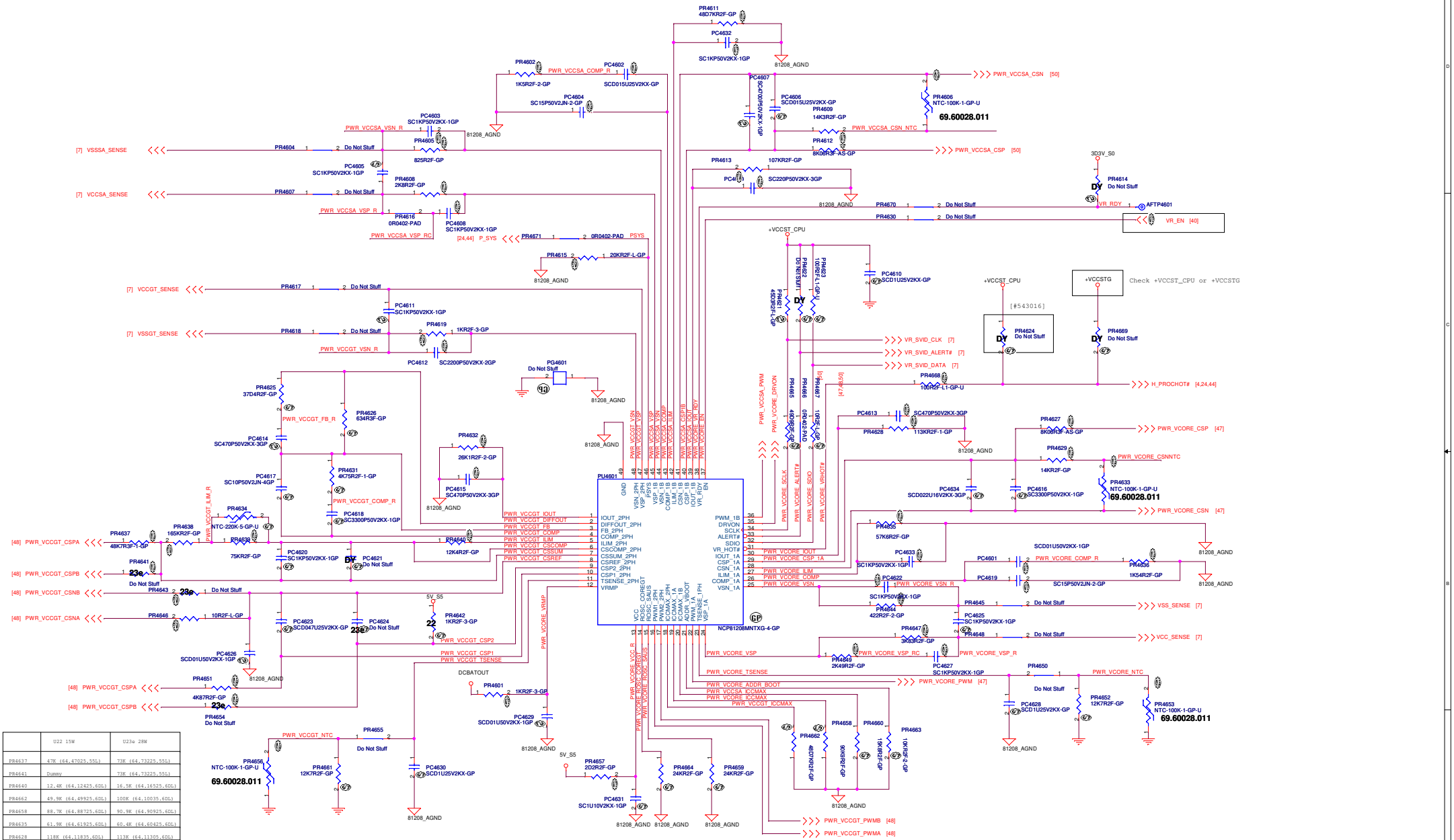
Main Func = CPU_CORE



	U22 15W	U23e 28W
PR4637	47K (64.47025.55L)	73K (64.73225.55L)
PR4641	Dummy	73K (64.73225.55L)
PR4640	12.4K (64.12425.6DL)	16.5K (64.16525.6DL)
PR4662	49.9K (64.49925.6DL)	100K (64.10035.6DL)
PR4658	88.7K (64.88725.6DL)	90.9K (64.90925.6DL)
PR4635	61.9K (64.61925.6DL)	60.4K (64.60425.6DL)
PR4628	118K (64.11835.6DL)	113K (64.11305.6DL)
PR4643	Dummy	10R (64.10R05.6DL)
PR4654	Dummy	4.87K (64.48715.6DL)
PC4624	Dummy	D047U (78.47322.2FL)
PR4642	1K (64.10015.6DL)	Dummy
PR4602	1.5K (64.15015.6DL)	10K (64.10025.6DL)
PC4602	15n (78.15322.2FL)	1kP (78.10224.2FL)

Iris SKL UMA

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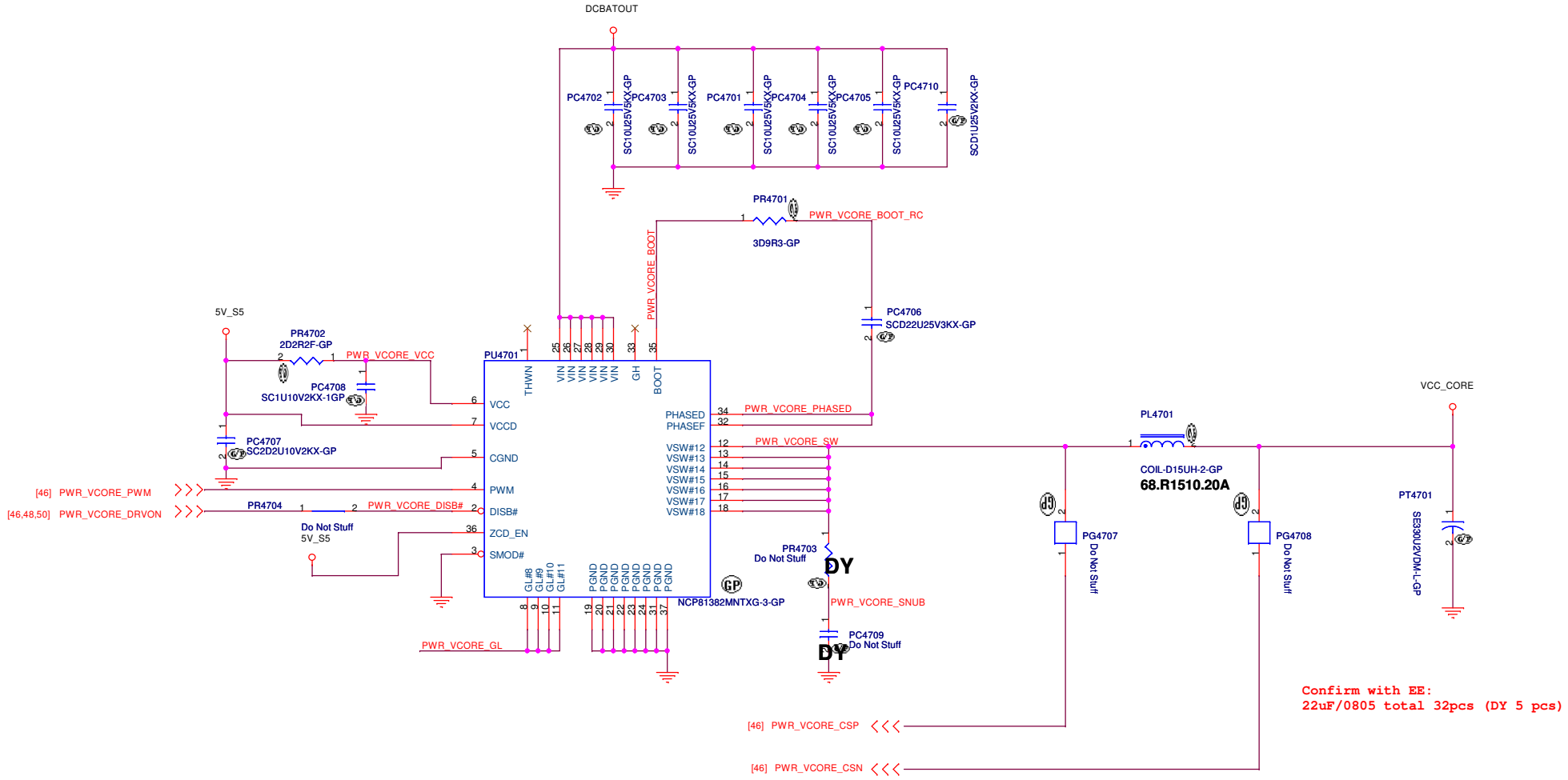
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81208MN_CPU_VCORE(1/3)

Size	Document Number	Rev
A2	Iris2 SKL-U	A00

Date: Wednesday, September 09, 2015 Sheet 46 of 105

Main Func = CPU_CORE



Iris SKL UMA

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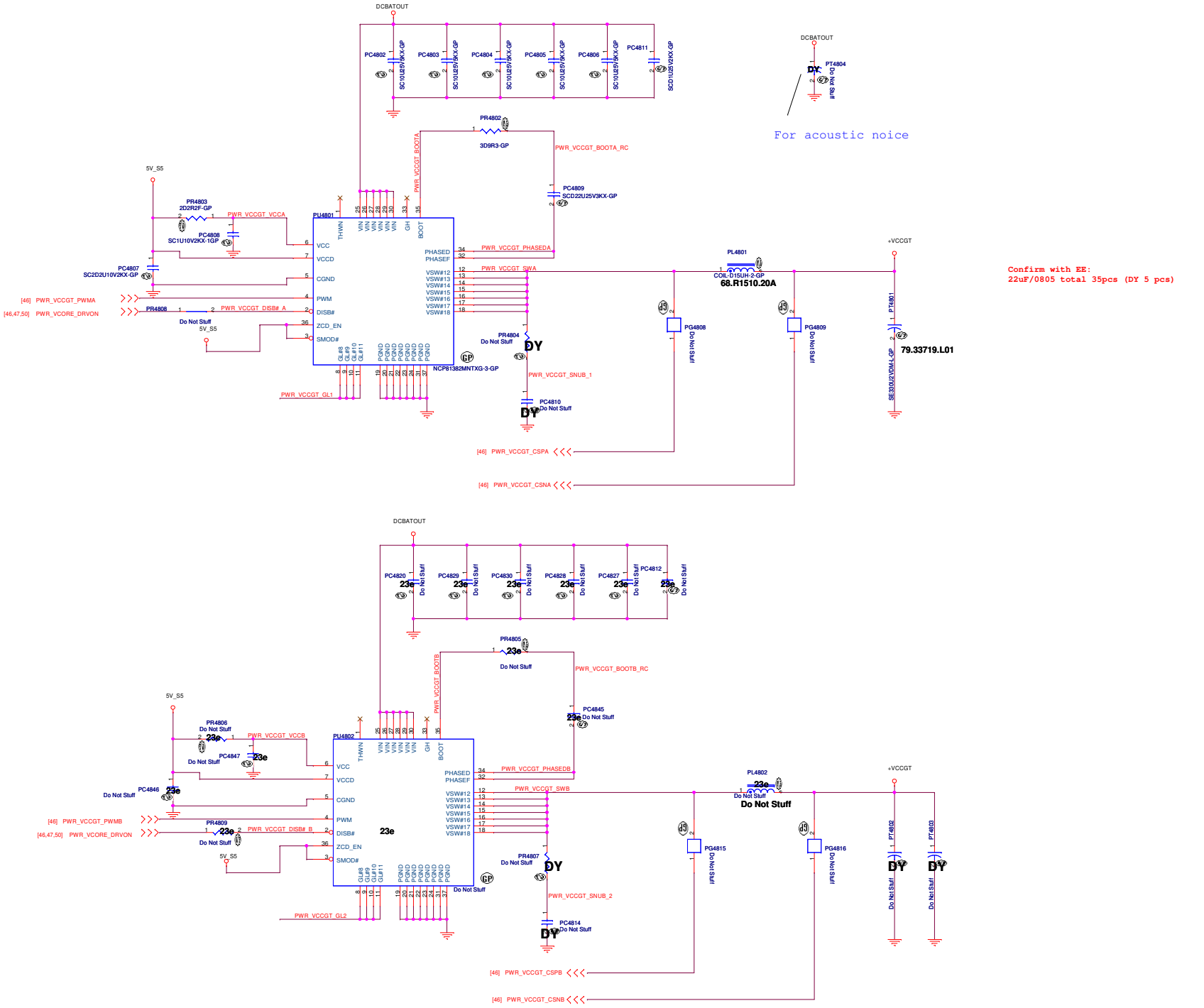
Taipei Hsien 221, Taiwan, R.O.C.

Title	NCP81382MN_CPU_VCORE(2/3)	
Size: A3	Document Number: Iris2 SKL-U	Rev: A00
Date: Wednesday, September 09, 2015	Sheet 47 of 105	

Main Func = CPU_CORE



Iris SKL UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCCGT(3/3)

Size: A2 | Document Number: Iris2 SKL-U | Rev: A00

Date: Wednesday, September 09, 2015 | Sheet 48 of 105

Iris SKL UMA

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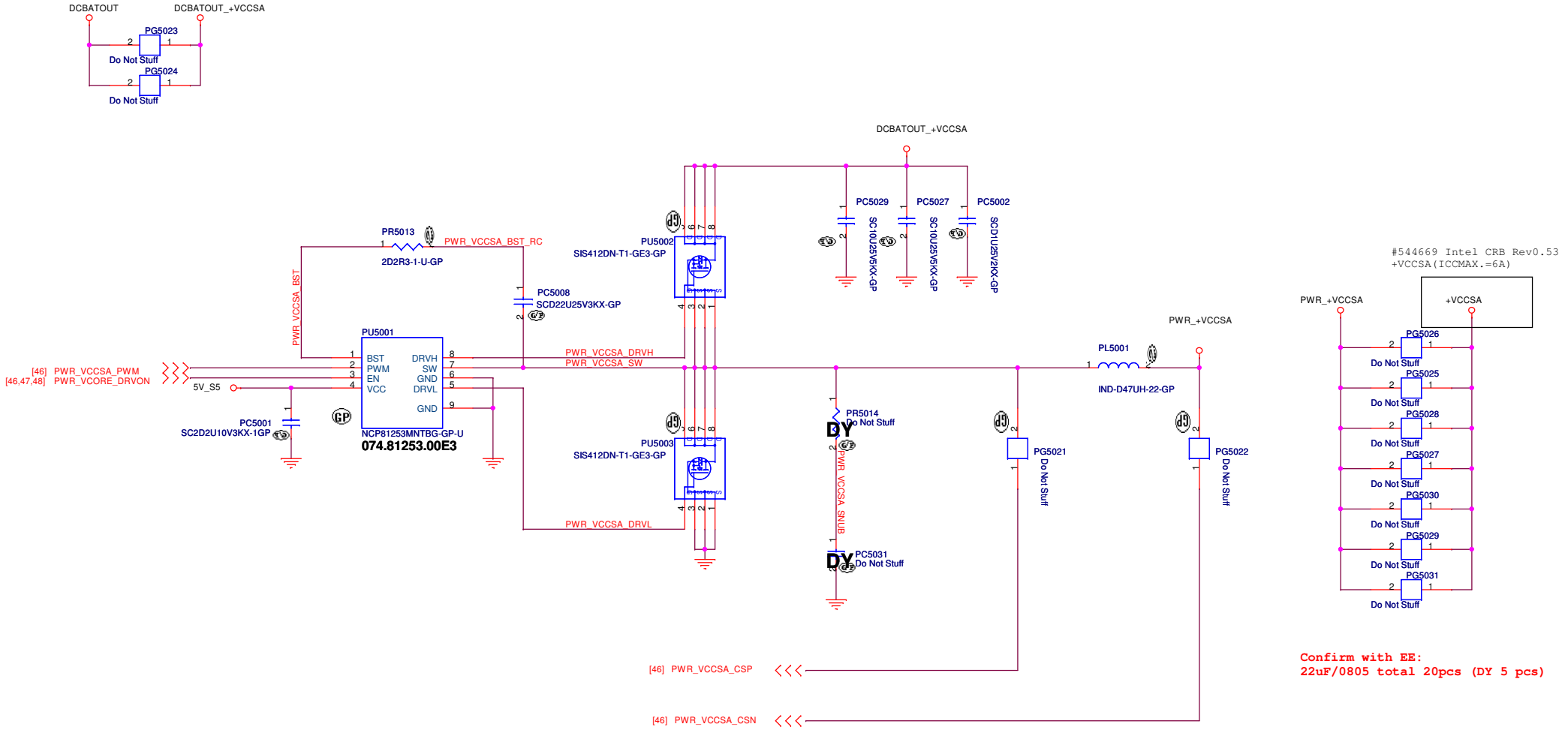
Title: NCP81210MN_CPU_VCCGTUS

Size: A2 | Document Number: Iris2 SKL-U | Rev: A00

Date: Tuesday, May 26, 2015 | Sheet 49 of 105

Main Func = CPU_CORE



#544669 Intel CRB Rev0.53
+VCCSA(ICCMAX.=6A)

Confirm with EE:
22uF/0805 total 20pcs (DY 5 pcs)

Iris SKL UMA

Wistron Corporation
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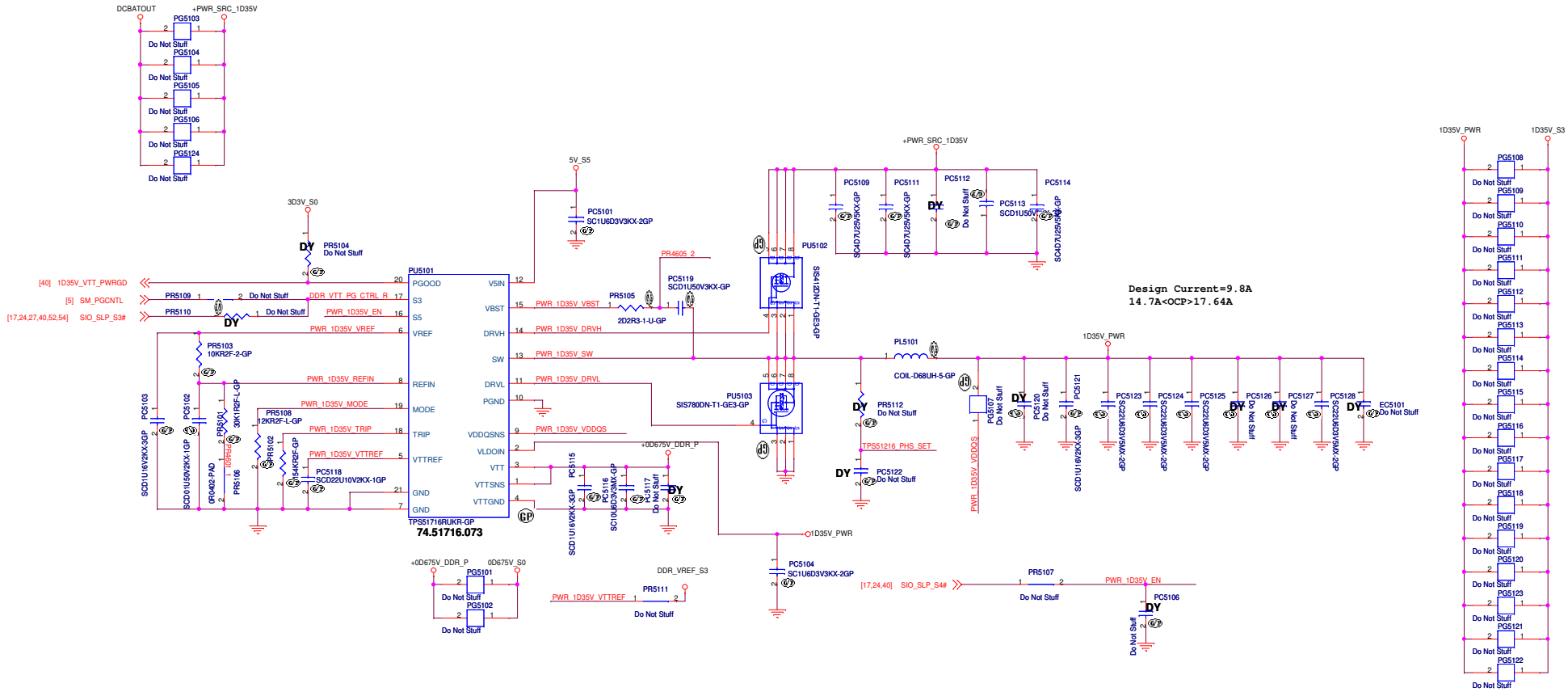
Title	NCP81253MN_CPU_VCCSA	
Size: A3	Document Number: Iris2 SKL-U	Rev: A00
Date: Wednesday, September 09, 2015	Sheet 50 of 105	

Main Func = VDDQ



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 0.68UH PCMC063T-R68 5~5.5mohm Isat =25Arms 68.R6810.20B
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R / 78.22610.51L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

20140728 david

Iris SKL UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MEM&MEMVTT

Size: C | Document Number: Iris2 SKL-U | Rev: A00

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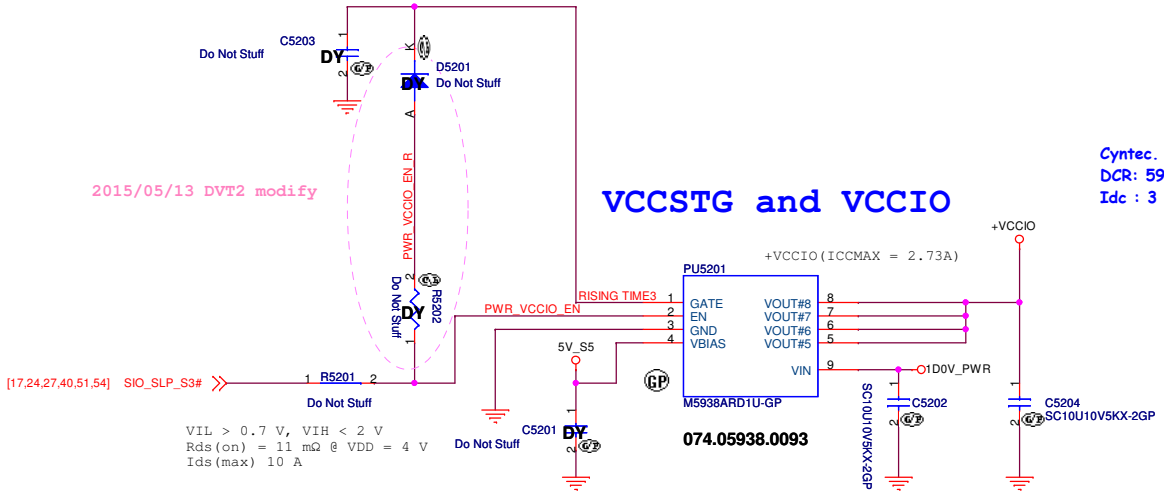
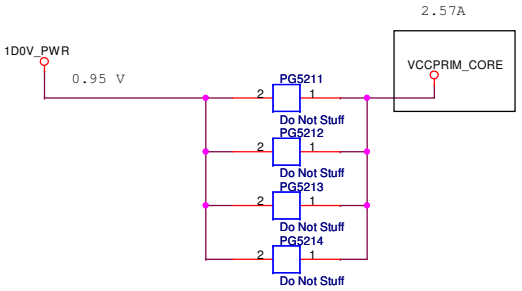
VCCIO



Power modify 2015/02/09

VCCPRIM_CORE

Design Current=1.8A
2.7A<OCP>3.24A



Iris SKL UMA

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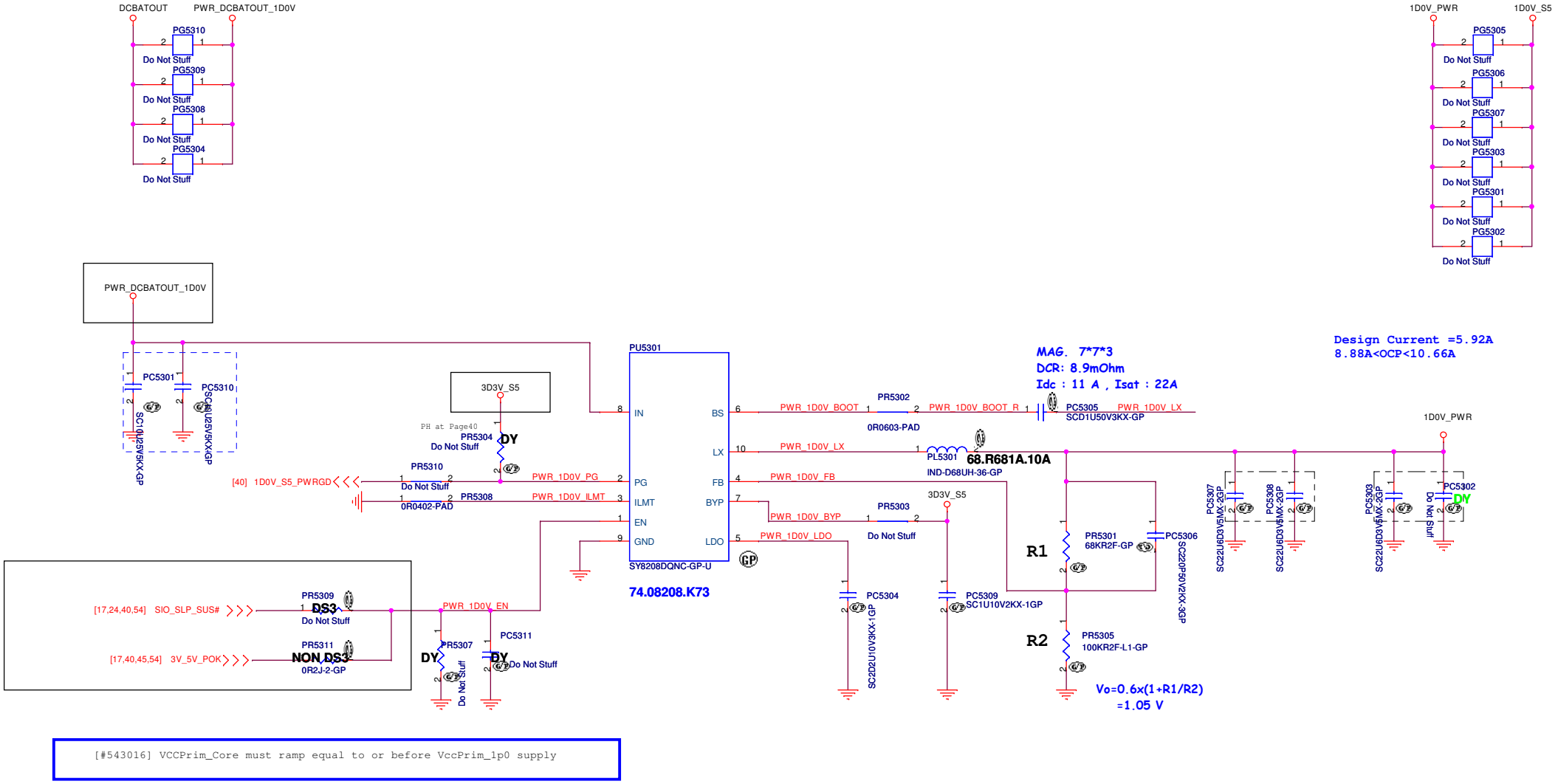
Taipei Hsien 221, Taiwan, R.O.C.

Title	DCDC-0D975V_VCCIO	
Size A3	Document Number Iris2 SKL-U	Rev A00
Date: Wednesday, September 09, 2015	Sheet 52 of 105	

Main Func = 1D0V



[#543016] VCCPrim_Core must ramp equal to or before VccPrim_1p0 supply

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 3.5Arms Chemi-con/ 79.3371V.6CL
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

Iris SKL UMA

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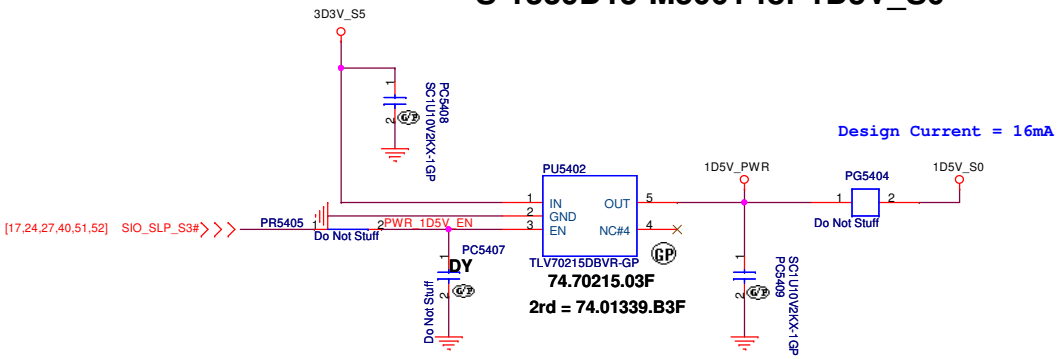
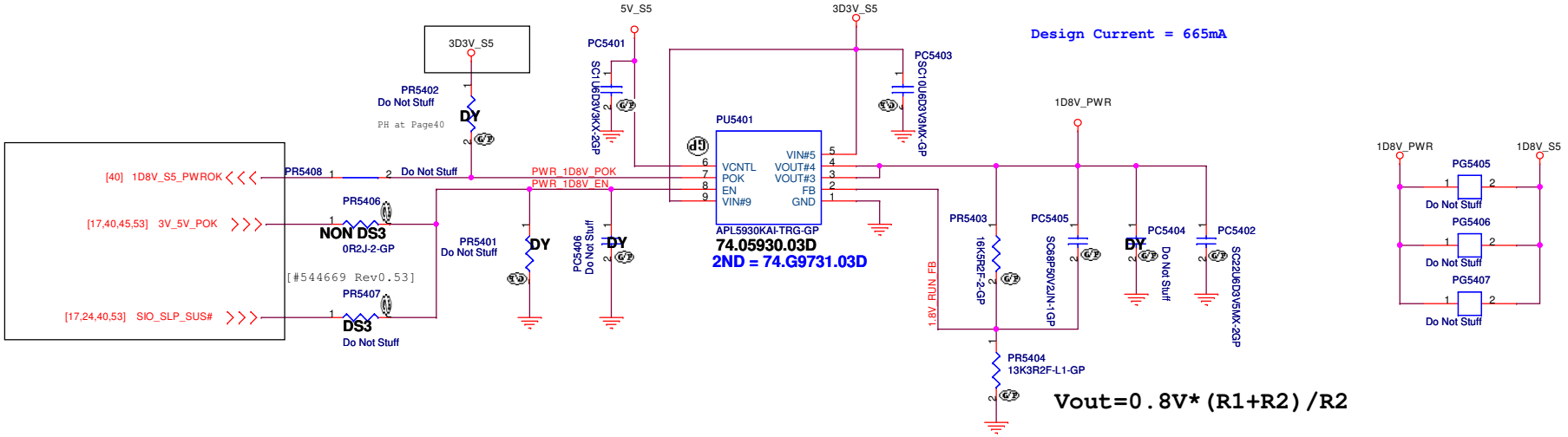
Title	DCDC-V1D00A		
Size A3	Document Number Iris2 SKL-U		Rev A00
Date: Wednesday, September 09, 2015	Sheet 53	of	105

Main Func = 1D5V

S-1339D15-M5001 for 1D5V_S0



APL5930 for 1D8V_S5



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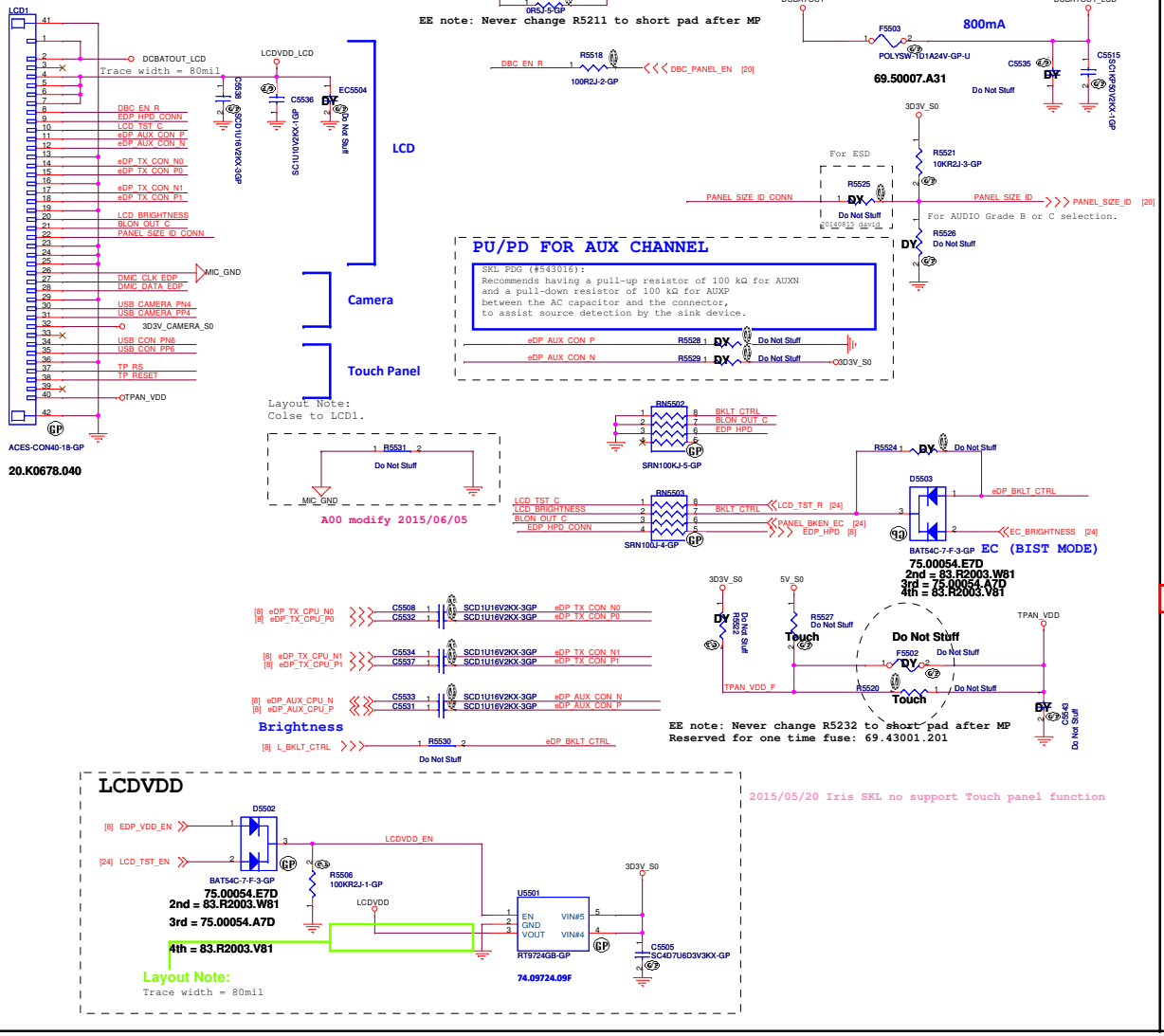
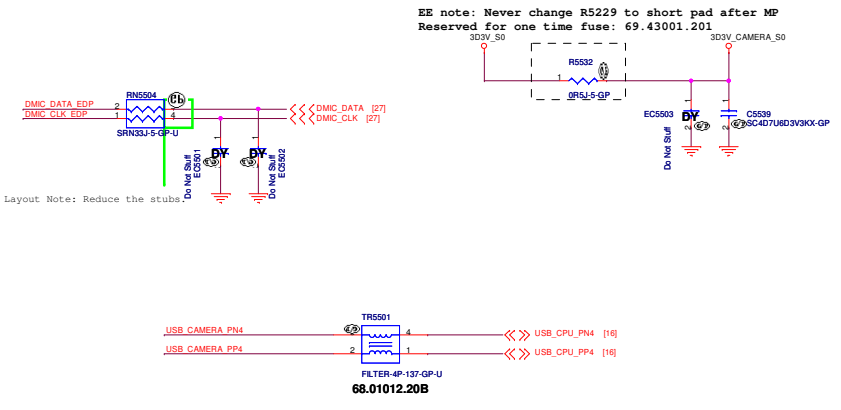
Title	LDO-V1D5V&V1D8V	
Size A3	Document Number Iris2 SKL-U	Rev A00
Date: Wednesday, September 09, 2015	Sheet 54 of 105	

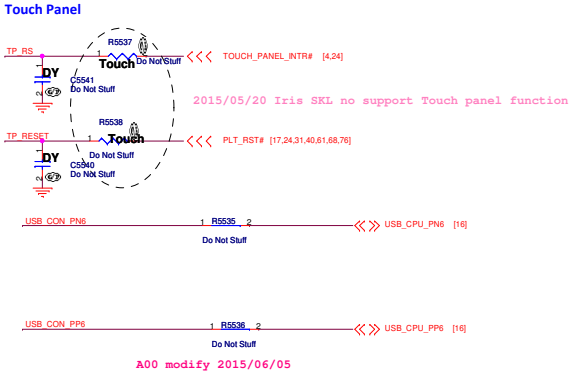
Main Func = LCD



Main Func = CAM



Main Func = TS



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Title: LCD&CAM&DMC&Touch

Size	Document Number	Rev
A2	Iris2 SKL-U	A00

Date: Wednesday, September 09, 2015 Sheet 55 of 105

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

		POL1_SDA(PIN22)	R/W
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

5V_HDMI_CRT_S0
5V_S0
R5409
Do Not Stuff
For DIODE in case of leakage from HDMI1
5V_HDMI_CRT_S0_R
F5501
POLYSW-1D1A6V-9-GP-U
D5501
Do Not Stuff
Do Not Stuff
69.48001.081
2ND = 69.50011.081
3RD = 69.50013.101

CRT RGB
CRT H/VSYNC
CRT SMBUS

X00_0425
CRT_DDCDATA_CON
CRT_HSYNC_CON
CRT_VSYNC_CON
CRT_DDCCLK_CON
C5516
C5513
C5507
C5511
Do Not Stuff
X00_0425

DP_CRT_R
DP_CRT_G
DP_CRT_B
L5503
L5501
L5502
2nd = 68.00245.011
CRT_R [57]
CRT_G [57]
CRT_B [57]
R5501
R5513
R5514
C5506
C5512
C5509
C5514
C5510
C5508
C5515
C5511
DP_CRT_HSYNC_CON
DP_CRT_VSYNC_CON
R5511
R5507
CRT_HSYNC_CON [57]
CRT_VSYNC_CON [57]
5V_HDMI_CRT_S0
RN5501
CRT_DDCDATA_CON
CRT_DDCCLK_CON

3D3V_S0
AVCC33
R5504
C5523
VDD_DAC_33
R5503
C5521

Layout note:
All cap need close to chip

U5502
AVCC_33
AVCC_12
DVCC_33
VCCK_12
VDD_DAC_33
LDO_EN
AUX_P
AUX_N
LANE0P
LANE0N
LANE1P
LANE1N
XI/CKIN
XO
RRX
HPD
SMB_SCL
SMB_SDA
VGA_SCL
VGA_SDA
VSYNC
HSYNC
RED_P
RED_N
GREEN_P
GREEN_N
BLUE_P
BLUE_N
POL1_SDA
POL2_SCL
GND_DAC
GND
CRT_PCH_HPD
PCH_SMBCLK [12,13,18,65,99]
PCH_SMBDATA [12,13,18,65,99]
CRT_DDCCLK_CON [57]
CRT_DDCDATA_CON [57]
DP_CRT_VSYNC_CON
DP_CRT_HSYNC_CON
DP_CRT_R
DP_CRT_G
DP_CRT_B
POL1_SDA
POL2_SCL
PCH_DPB_AUXP
PCH_DPB_AUXN
HDMI_CRT_P0
HDMI_CRT_N0
HDMI_CRT_P1
HDMI_CRT_N1
PCH_DPC_AUXP_U
PCH_DPC_AUXN_U
PCH_DPC_P0_U
PCH_DPC_N0_U
PCH_DPC_P1_U
PCH_DPC_N1_U
CLK_DP2VGA
CLK_XO
R5519
R5505
Do Not Stuff
R5517
R5510
CPU_DP1_HPD [8,57]
X00_0505
X00_0429
AFTP5501
AFTP5502
AFTP5503
AFTP5504
AFTP5505
AFTP5506
AFTP5507
AFTP5508

X00_0428
R5509
R5515
R5508
R5516
POL1_SDA
POL2_SCL

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

R5502
R5512
LDO_EN

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

U5504
A0
A1
A2
VSS
WP
SCL
SDA
VCC
POL2_SCL
POL1_SDA

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

1	0	1	0	A_2	A_1	A_0	R/W

DEVICE ADDRESS

Figure 3. Slave Address Bits

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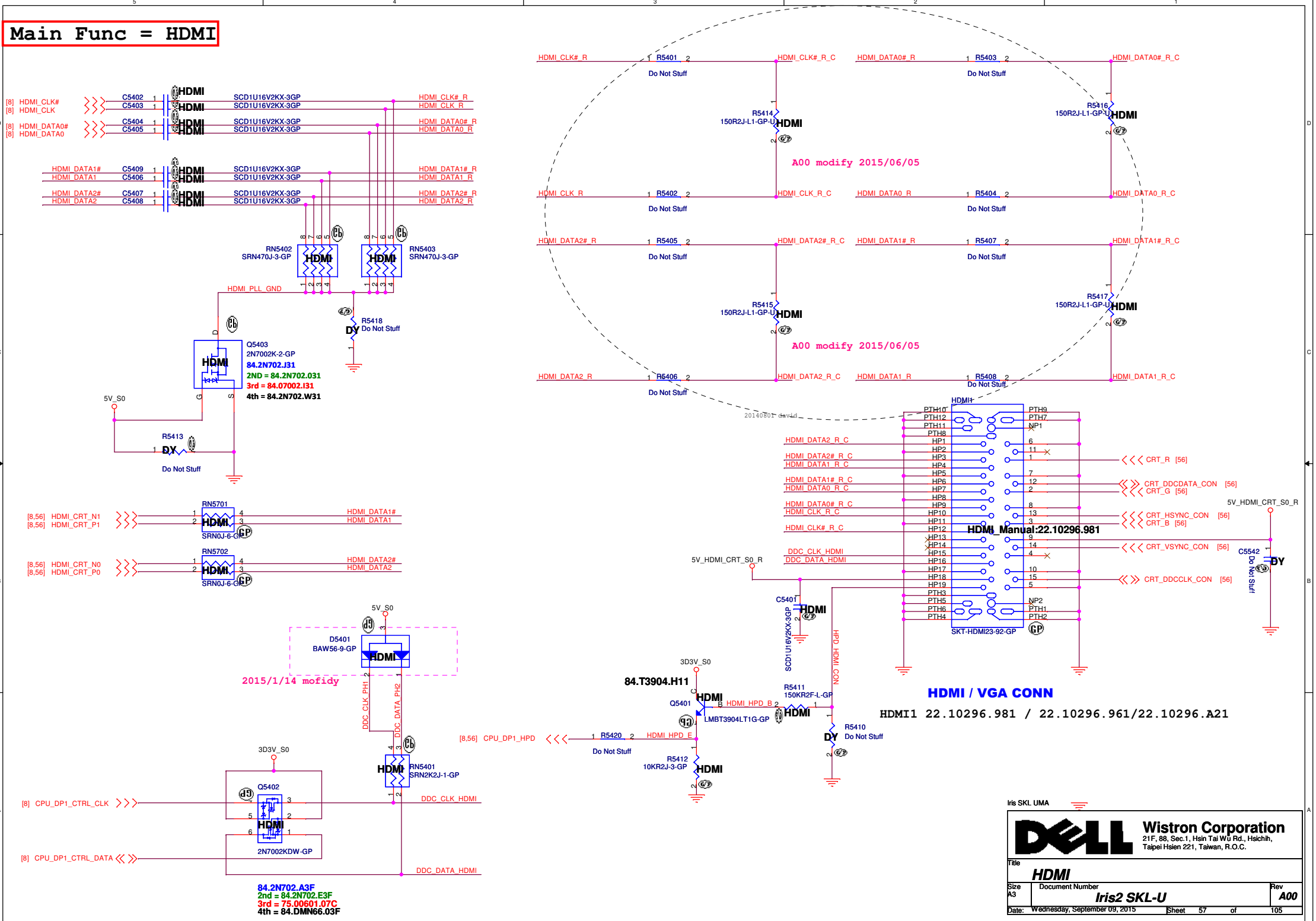
Title: CRT
Size: A2
Document Number: Iris2 SKL-U
Rev: A00
Date: Wednesday, September 09, 2015
Sheet 56 of 105

Main Func = HDMI



Iris SKL UMA

DELL

Wistron Corporation
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Title	*HDMI*	
Size A3	Document Number *Iris2 SKL-U*	Rev *A00*
Date: Wednesday, September 09, 2015	Sheet 57 of 105	

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Title: *(Reserved)*

Size: A3 | Document Number: *Iris2 SKL-U* | Rev: *A00*

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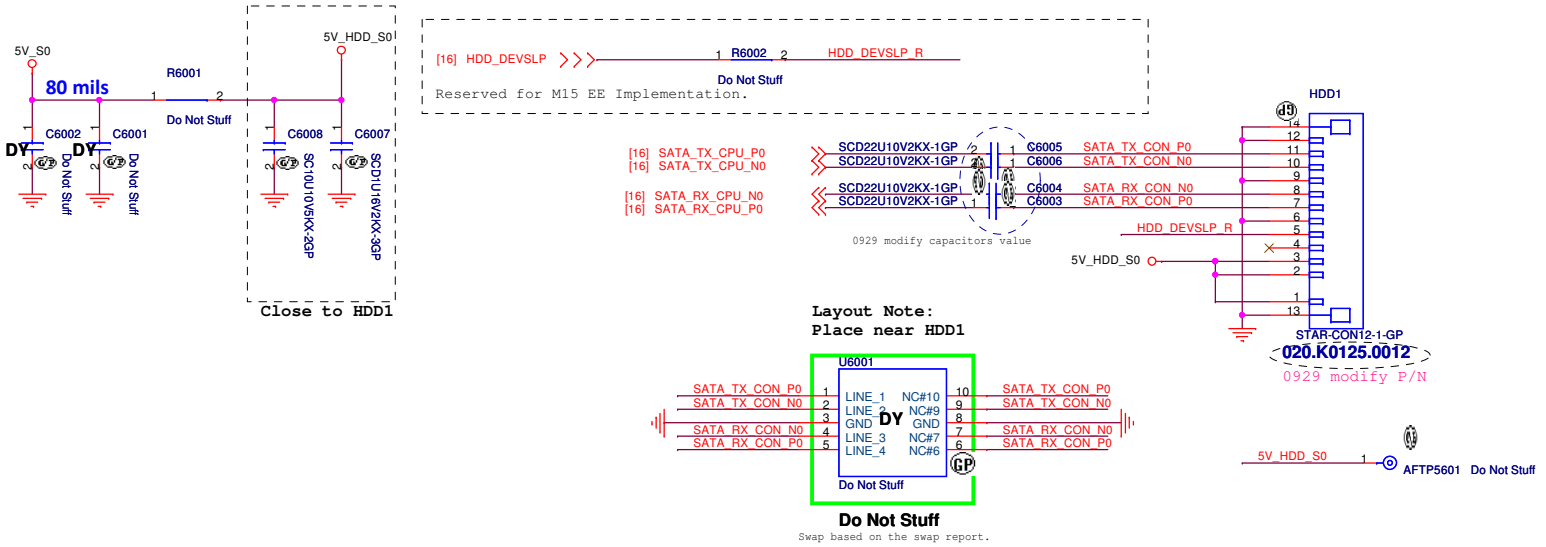
Title: *(Reserved)*

Size: A3 | Document Number: *Iris2 SKL-U* | Rev: *A00*

Date: Tuesday, May 26, 2015 | Sheet 59 of 105

Main Func = HDD

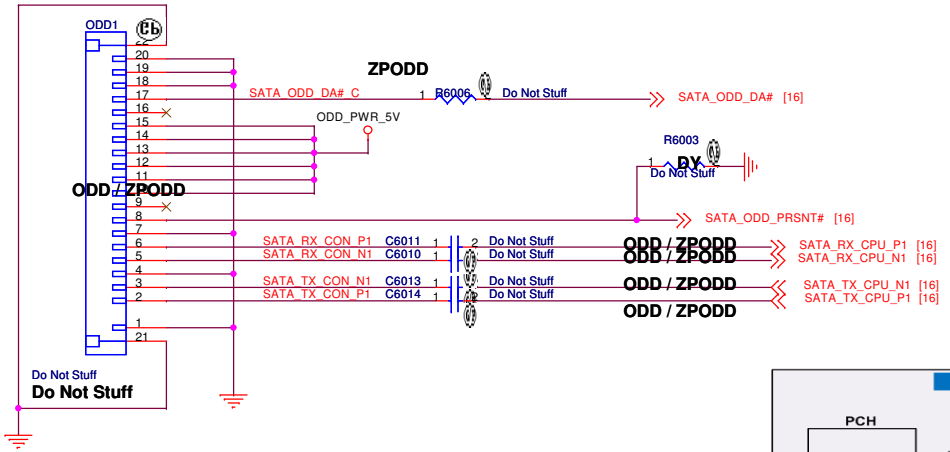
SATA HDD Connector



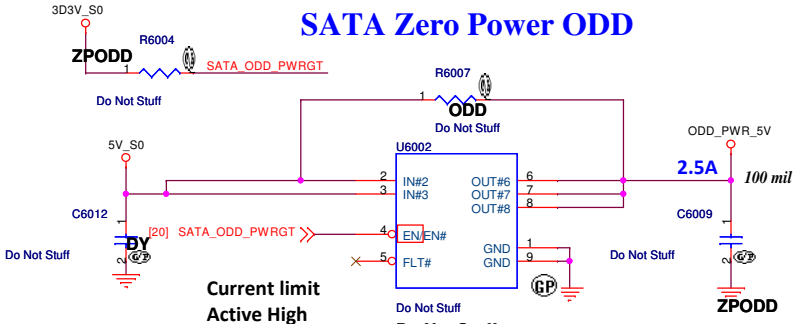
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

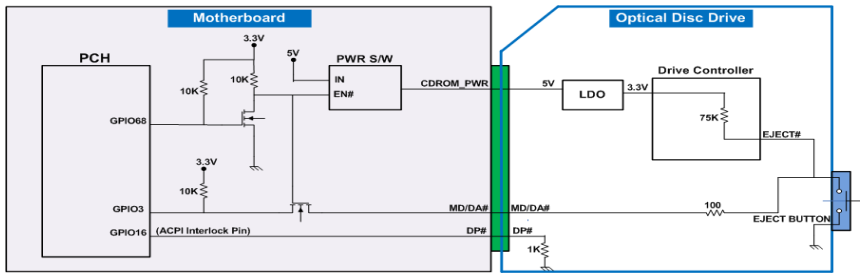
ODD Connector



SATA Zero Power ODD



74.02001.079 is OBS
Will use 74.06288.079
but 74.06288.079 is also OBS
we will use 074.06288.0079.



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Title: SATA IF_HDD/ODD

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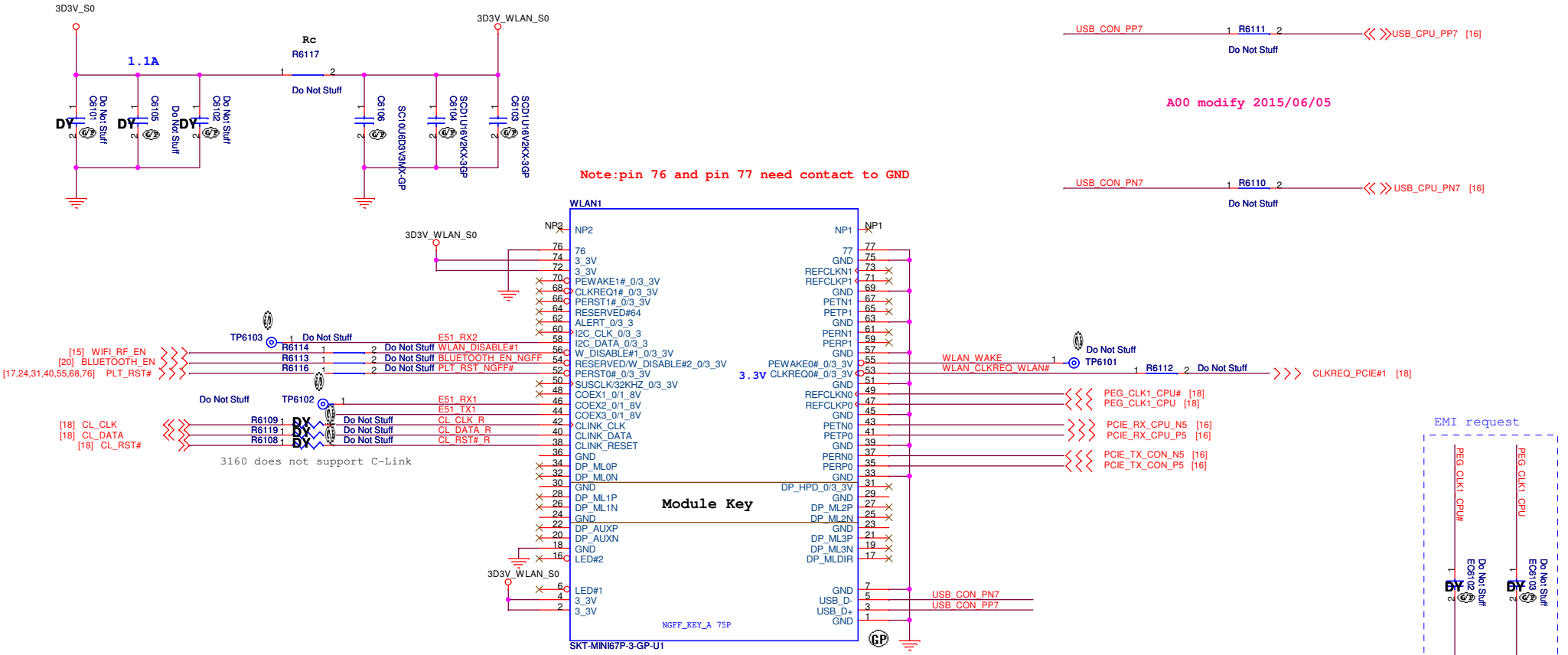
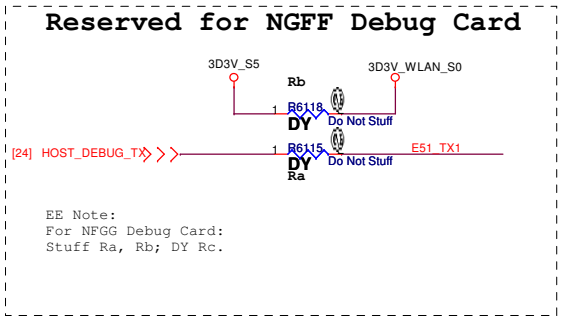
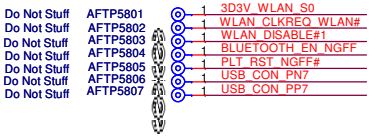
Main Func = WLAN



Support: Intel Dual Band Wireless-AC 3160





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Title	NGFF WLAN CONN	
Size A3	Document Number Iris2 SKL-U	Rev A00
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Title: *Reserved*

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Iris2 SKL-U*	*A00*

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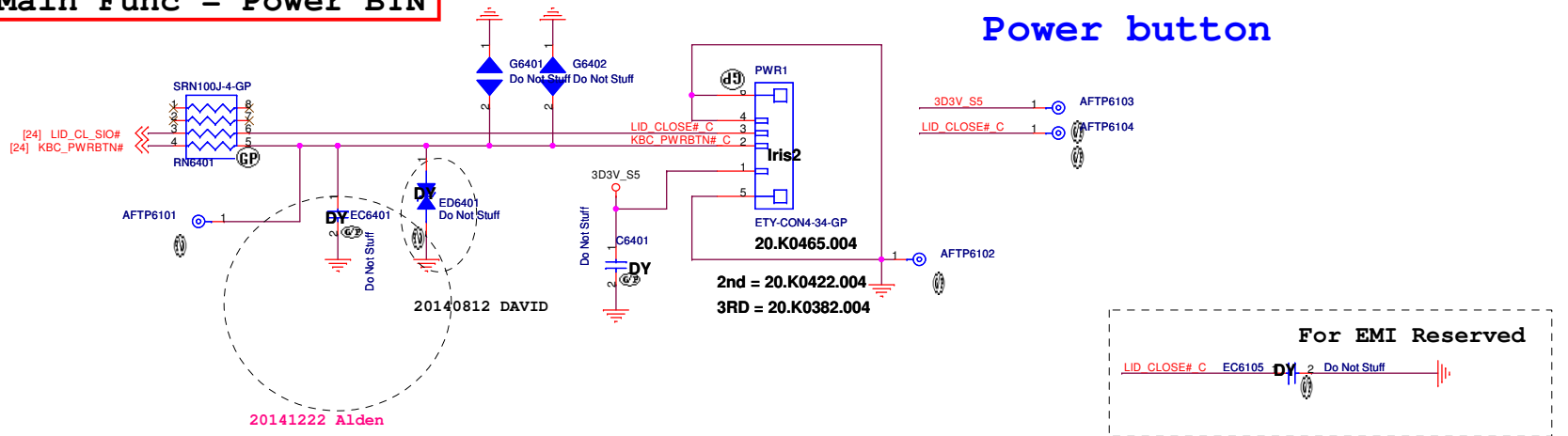
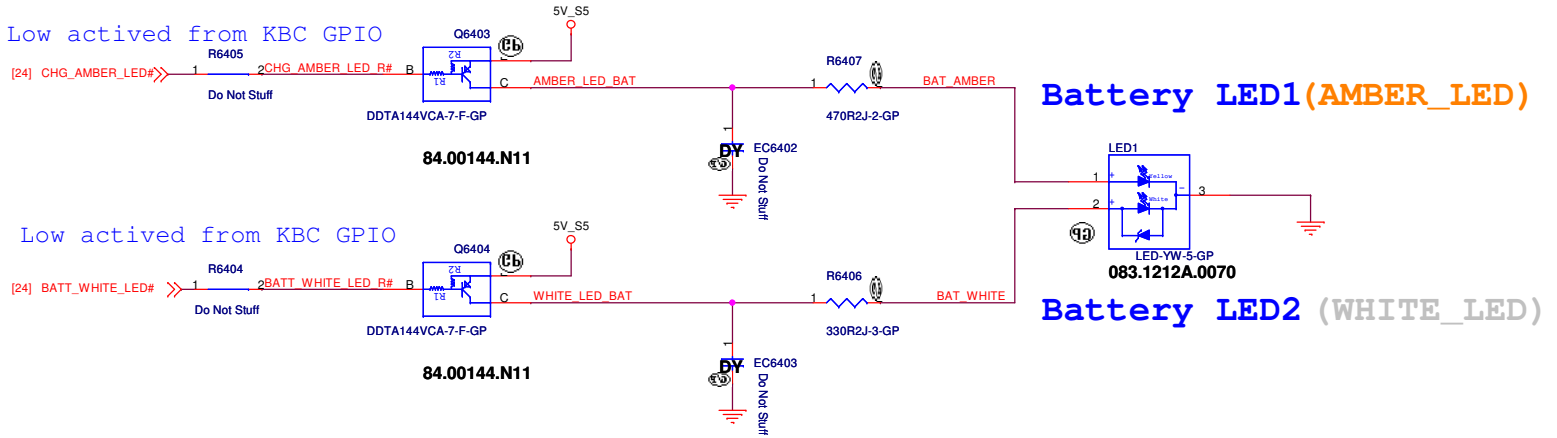
Main Func = Power BTN

Power button

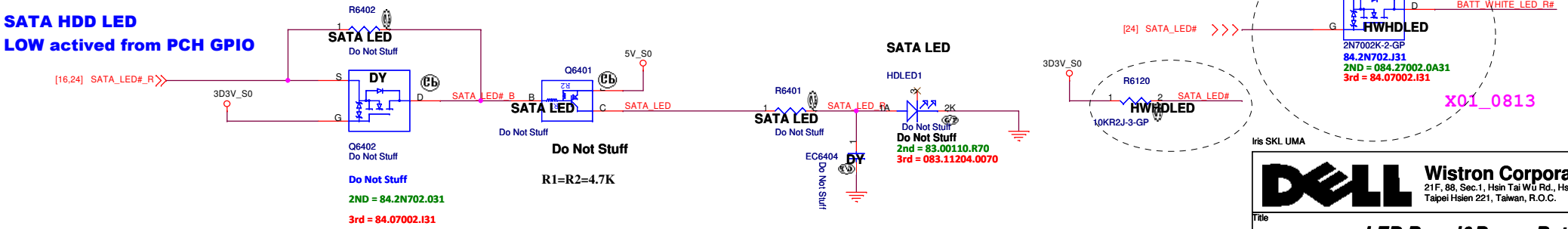


For EMI Reserved

Main Func = Battery LED



Main Func = HDD LED



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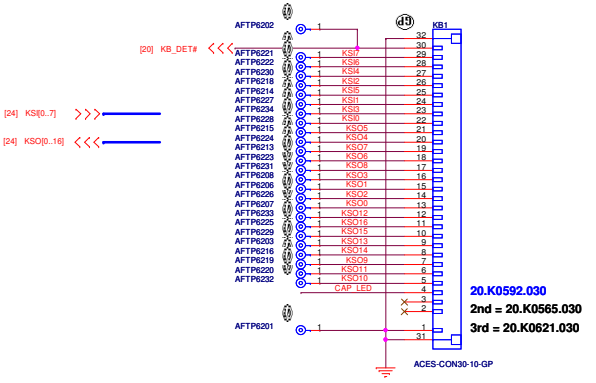
Title	LED Board&Power Button	
Size A3	Document Number Iris2 SKL-U	Rev A00
Date: Wednesday, September 09, 2015	Sheet 64 of 105	

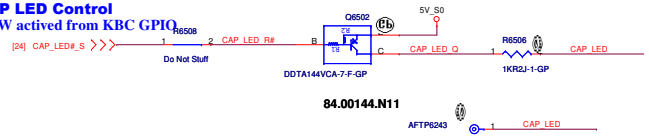
Main Func = KB

Internal Keyboard Connector

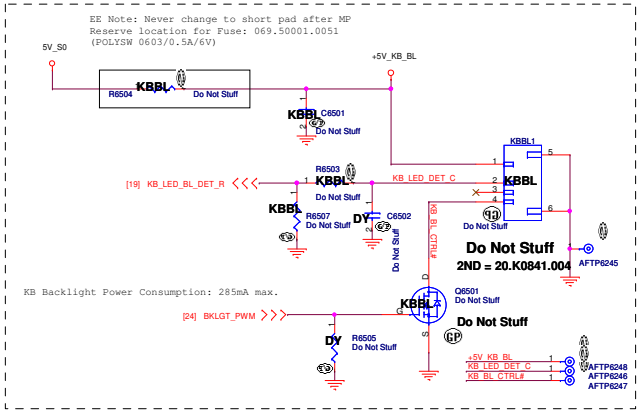


CAP LED Control

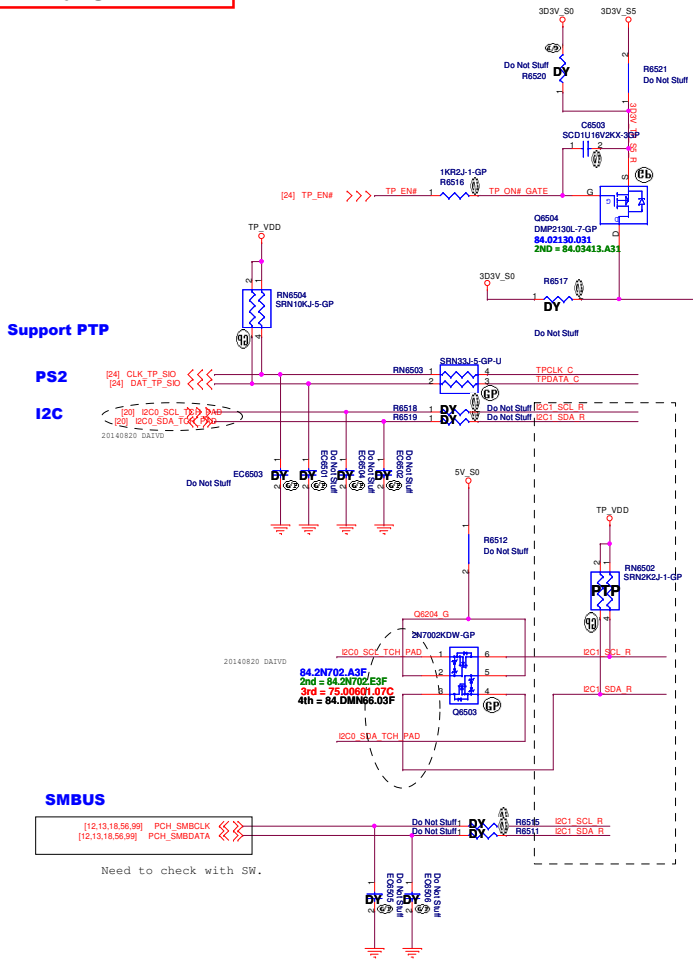
LOW actived from KBC GPIO

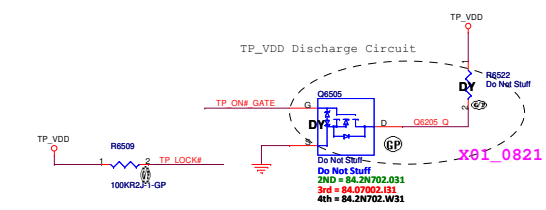


Keyboard Backlight (Reserved)

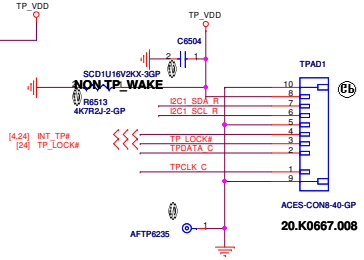


Main Func = TPAD



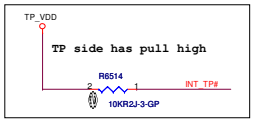


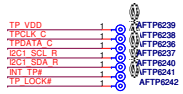
Precision Touch Pad Connector



Pin number	Pin name
8	VDD
7	DAT(I2C)
6	CLK(I2C)
5	GND
4	ATTN
3	GPIO
2	DAT(PS2)
1	CLK(PS2)

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.





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Title: Key Board&Touch Pad

Size: A2 | Document Number: Iris2 SKL-U | Rev: A00

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Main Func = IO Connector

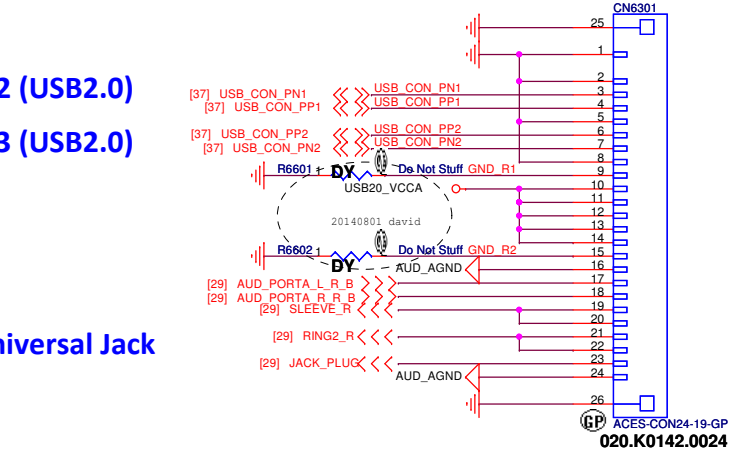
I/O Board Connector

connector follow IRIS2

USB2 (USB2.0)

USB3 (USB2.0)

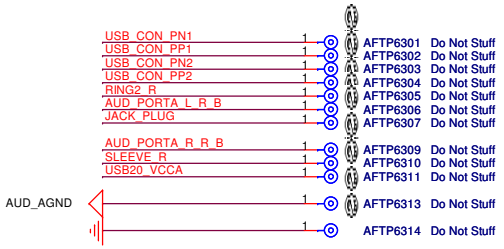
Universal Jack



020.K0142.0024

2rd = 020.K0139.0024

Pitch: 1mm
Power: 5 pins
GND: 4 pins
AGND: 2 Pins



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Title: IO Board Connector

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Title: *Reserved*

Size: A3 | Document Number: *Iris2 SKL-U* | Rev: *A00*

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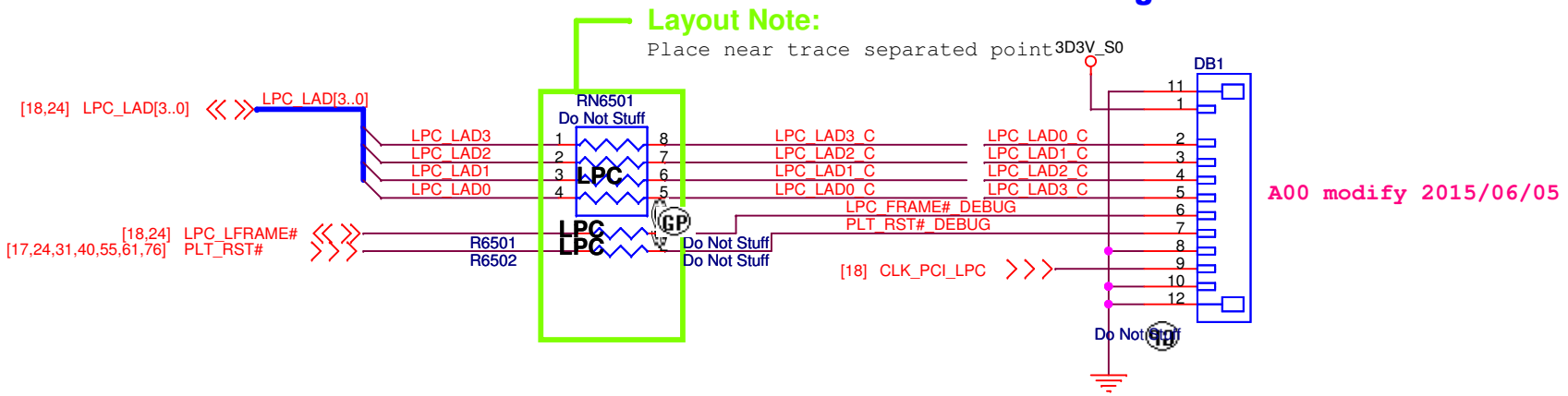
Main Func = Debug

Debug Connector



A00 modify 2015/06/05

20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

Iris SKL UMA

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Title: *Dubug connector*		
Size: A4	Document Number: *Iris2 SKL-U*	Rev: *A00*
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Title: *Reserved*

Size	Document Number	Rev
A3	*Iris2 SKL-U*	*A00*

Main Func = Hall Sensor

(Blanking)

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Title

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Title: *RESERVED*

Size: A3 | Document Number: *Iris2 SKL-U* | Rev: *A00*

Date: Tuesday, May 26, 2015 | Sheet 71 of 105

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Title

USB3.0 PORT

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Title: *Reserved*

Size: A3 | Document Number: *Iris2 SKL-U* | Rev: *A00*

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Title

Reserved

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Title: *Reserved*

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Date: Tuesday, May 26, 2015 Sheet 75 of 105

GFX & GPP, 85Ω
GFX & GPP CLK, 85Ω

GPU1A 1 OF 7

Table 3–5 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTb	I	Fundamental reset. 3.3-V tolerant pad. This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (± 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to a 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to a 8.0-GT/s bit rate.
PCIE_CALR_RX	I	Connect to PCIE_VDDC through a 1-kΩ (1% tolerance) resistor.
PCIE_CALR_TX	I	Connect to PCIE_VDDC through a 1.69-kΩ (1% tolerance) resistor.
CLKREQB	O	Reserved, do not connect on the PCB.

DGPU_HOLD_RST#	
H	dGPU mode
L	IGPU
H	IGPU with BACO

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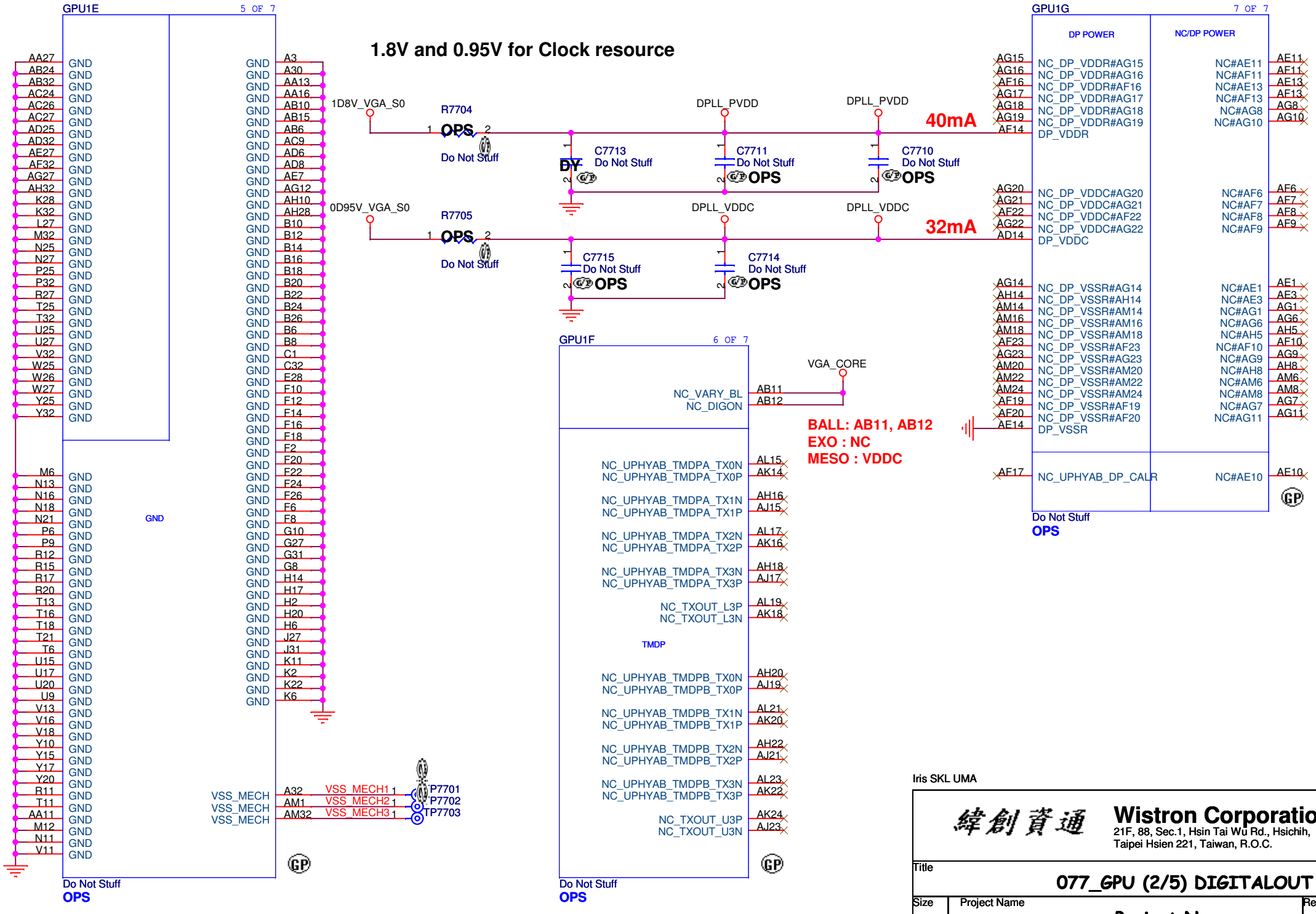
Title: 076_GPU(1/5) PEG
Size: Project Name: <Project Name> Rev: SA
Date: Wednesday, September 09, 2015 Sheet 76 of 105



Iris SKL UMA

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Taipei Hsien 221, Taiwan, R.O.C.

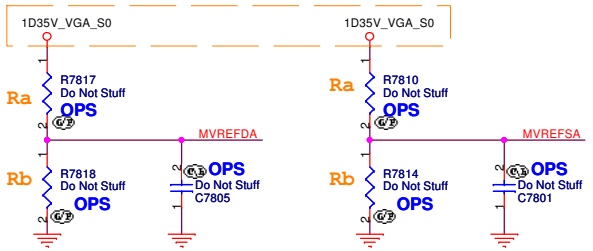
Title	077_GPU (2/5) DIGITALOUT	
Size	Project Name <Project Name>	Rev SA
Date: Tuesday, May 26, 2015	Sheet 77 of 105	

Signal GRP	Signal			
Clocks	CLK			
Address	ADD	BANK		
Command	RAS_L	CAS_L	WE_L	
Control	CKE	ODT	CS_L	
Data	Data	CHECK	DM	DQS

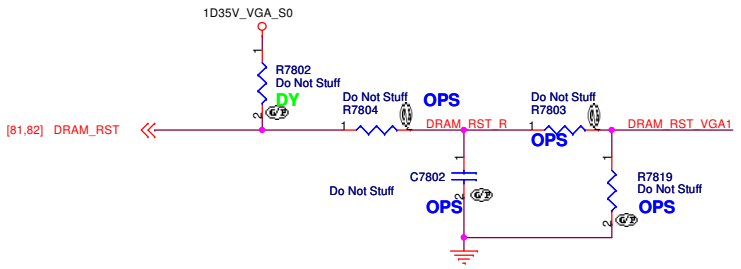
Please MVREF drivers and Caps close to ASIC

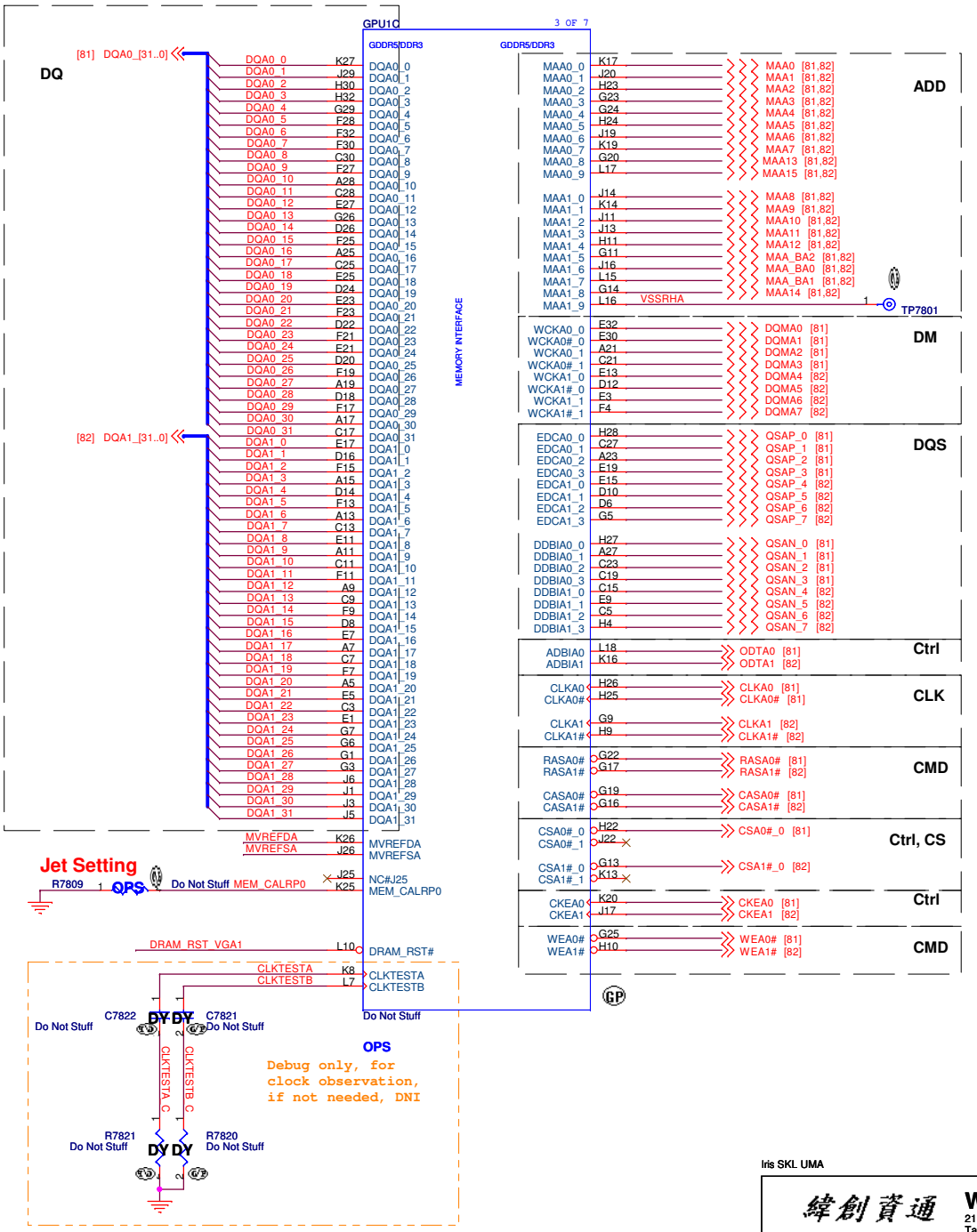
DDR3/GDDR3 Memory Stuff Option(JET/TOPAZ)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



Place all these componets very close to GPU (within 25mm) and keep all components close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5





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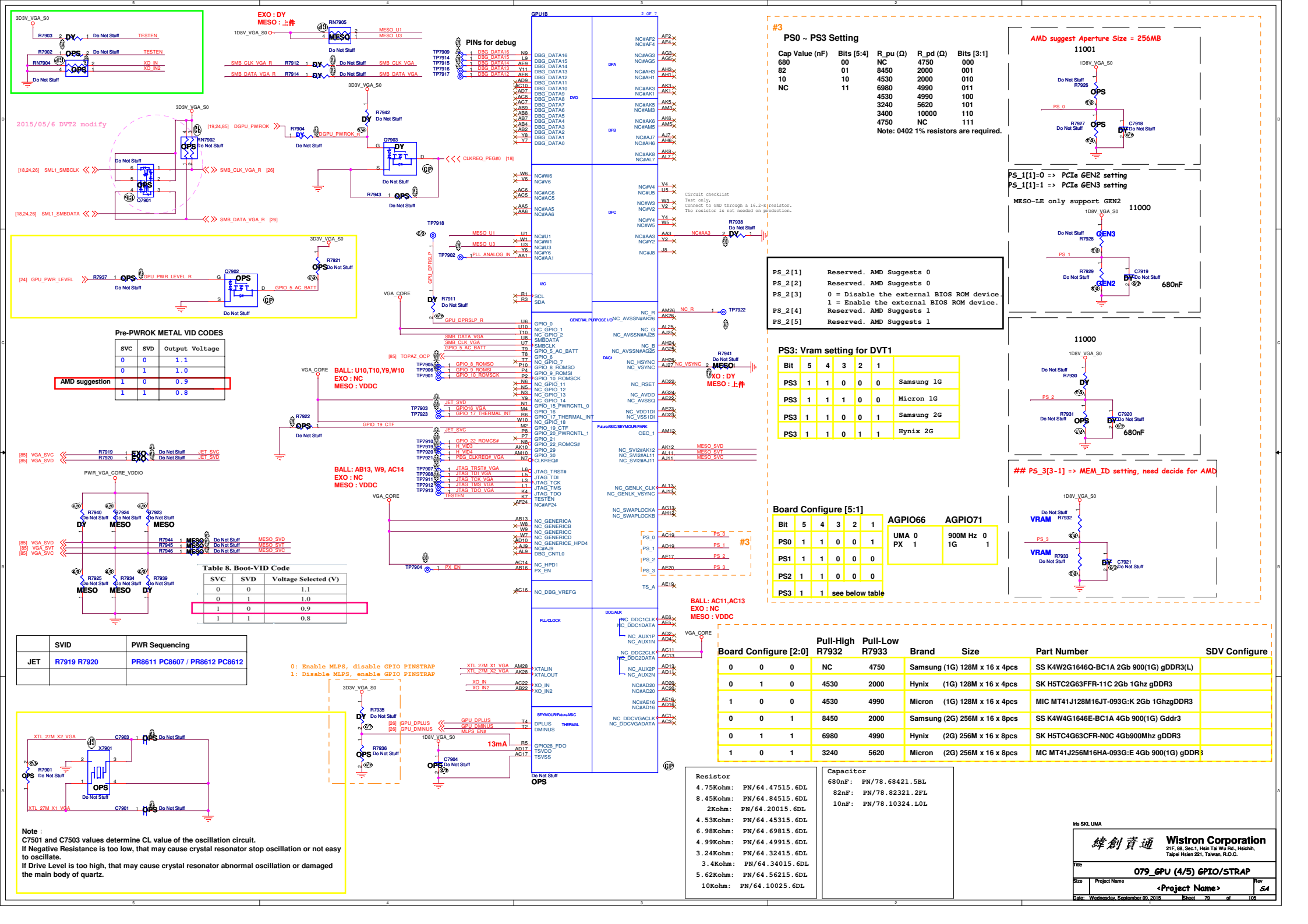
Taipei Hsien 221, Taiwan, R.O.C.

Title: 078_GPU (3/5) VRAM I/F

Size | Project Name: <Project Name> | Rev: SA

Date: Wednesday, September 09, 2015 | Sheet 78 of 105


EXO : DY
MESO : 上件
PINs for debug
2015/05/6 DVT2 modify
Pre-PWROK METAL VID CODES
SVC SVD Output Voltage
0 0 1.1
0 1 1.0
AMD suggestion 1 0 0.9
1 1 0.8
BALL: U10,T10,Y9,W10
EXO : NC
MESO : VDDC
BALL: AB13, W9, AC14
EXO : NC
MESO : VDDC
BALL: AC11,AC13
EXO : NC
MESO : VDDC
Table 8. Boot-VID Code
SVC SVD Voltage Selected (V)
0 0 1.1
0 1 1.0
1 0 0.9
1 1 0.8
SVID PWR Sequencing
JET R7919 R7920 PR8611 PC8607 / PR8612 PC8612
0: Enable MLPS, disable GPIO PINSTRAP
1: Disable MLPS, enable GPIO PINSTRAP
13mA
Note :
C7501 and C7503 values determine CL value of the oscillation circuit.
If Negative Resistance is too low, that may cause crystal resonator stop oscillation or not easy to oscillate.
If Drive Level is too high, that may cause crystal resonator abnormal oscillation or damaged the main body of quartz.
#3
PS0 ~ PS3 Setting
Cap Value (nF) Bits [5:4] R_pu (Ω) R_pd (Ω) Bits [3:1]
680 00 NC 4750 000
82 01 8450 2000 001
10 10 4530 2000 010
NC 11 6980 4990 011
4530 4990 100
3240 5620 101
3400 10000 110
4750 NC 111
Note: 0402 1% resistors are required.
PS_2[1] Reserved. AMD Suggests 0
PS_2[2] Reserved. AMD Suggests 0
PS_2[3] 0 = Disable the external BIOS ROM device.
1 = Enable the external BIOS ROM device.
PS_2[4] Reserved. AMD Suggests 1
PS_2[5] Reserved. AMD Suggests 1
PS3: Vram setting for DVT1
Bit 5 4 3 2 1
PS3 1 1 0 0 0 Samsung 1G
PS3 1 1 1 0 0 Micron 1G
PS3 1 1 0 0 1 Samsung 2G
PS3 1 1 0 1 1 Hynix 2G
Board Configure [5:1]
Bit 5 4 3 2 1
PS0 1 1 0 0 1
PS1 1 1 0 0 0
PS2 1 1 0 0 0
PS3 1 1 see below table
AGPIO66 AGPIO71
UMA 0 900M Hz 0
PX 1 1G 1
AMD suggest Aperture Size = 256MB
11001
PS_1[1]=0 => PCIe GEN2 setting
PS_1[1]=1 => PCIe GEN3 setting
MESO-LE only support GEN2
11000
11000
680nF
680nF
PS_3[3-1] => MEM_ID setting, need decide for AMD
Board Configure [2:0] Pull-High R7932 Pull-Low R7933 Brand Size Part Number SDV Configure
0 0 0 NC 4750 Samsung (1G) 128M x 16 x 4pcs SS K4W2G1646Q-BC1A 2Gb 900(1G) gDDR3(L)
0 1 0 4530 2000 Hynix (1G) 128M x 16 x 4pcs SK H5TC2G63FFR-11C 2Gb 1Ghz gDDR3
1 0 0 4530 4990 Micron (1G) 128M x 16 x 4pcs MIC MT41J128M16JT-093G:K 2Gb 1GhzgDDR3
0 0 1 8450 2000 Samsung (2G) 256M x 16 x 8pcs SS K4W4G1646E-BC1A 4Gb 900(1G) Gddr3
0 1 1 6980 4990 Hynix (2G) 256M x 16 x 8pcs SK H5TC4G63CFR-N0C 4Gb900Mhz gDDR3
1 0 1 3240 5620 Micron (2G) 256M x 16 x 8pcs MC MT41J256M16HA-093G:E 4Gb 900(1G) gDDR3
Resistor
4.75Kohm: PN/64.47515.6DL
8.45Kohm: PN/64.84515.6DL
2Kohm: PN/64.20015.6DL
4.53Kohm: PN/64.45315.6DL
6.98Kohm: PN/64.69815.6DL
4.99Kohm: PN/64.49915.6DL
3.24Kohm: PN/64.32415.6DL
3.4Kohm: PN/64.34015.6DL
5.62Kohm: PN/64.56215.6DL
10Kohm: PN/64.10025.6DL
Capacitor
680nF: PN/78.68421.5BL
82nF: PN/78.82321.2FL
10nF: PN/78.10324.L0L
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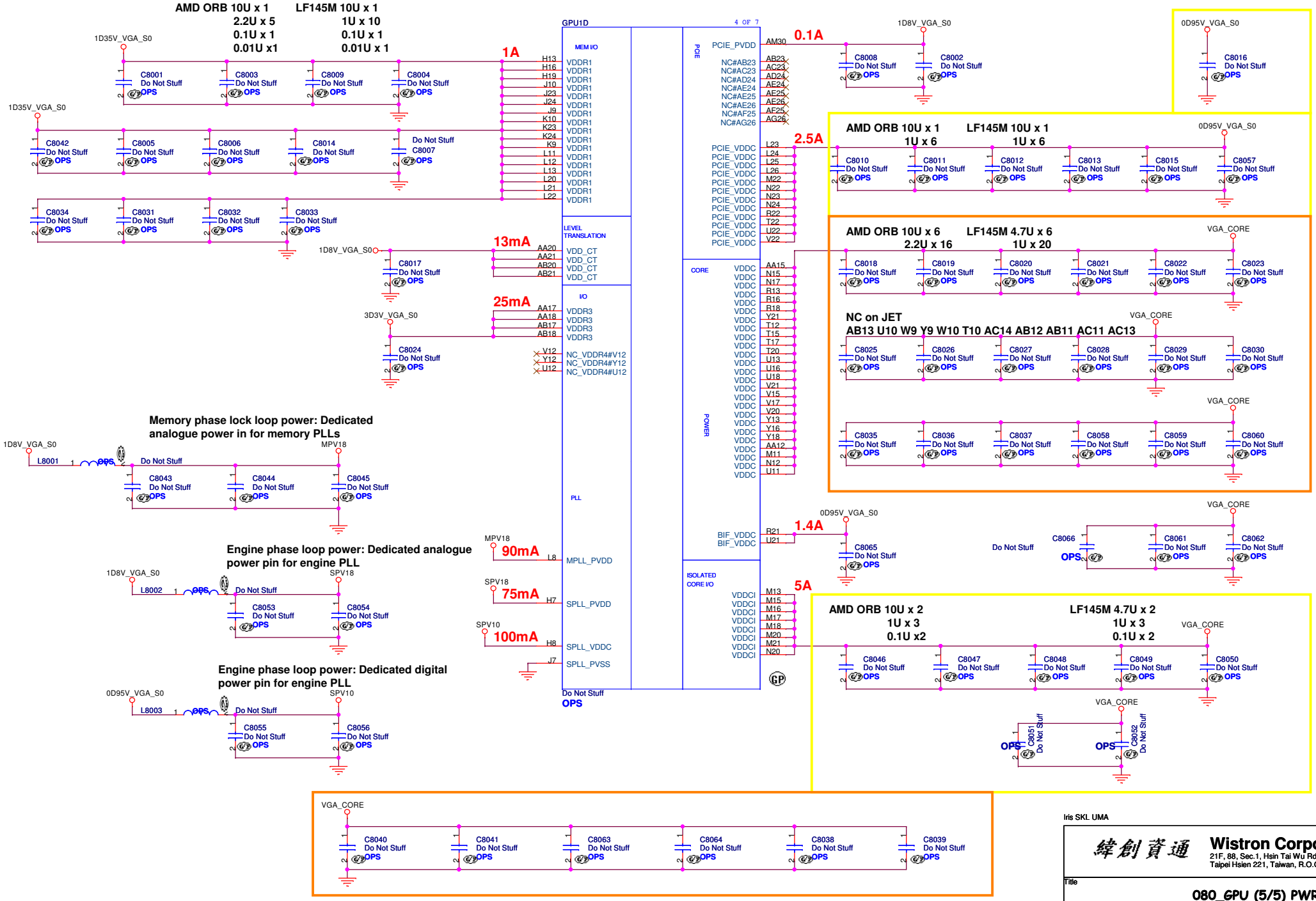
079_GPU (4/5) GPIO/STRAP
<Project Name>
Wednesday, September 09, 2015


AMD ORB 10U x 1
2.2U x 5
0.1U x 1
0.01U x1
LF145M 10U x 1
1U x 10
0.1U x 1
0.01U x 1
1D35V_VGA_S0
1A
GPU1D
4 OF 7
MEM I/O
LEVEL TRANSLATION
I/O
PLL
PCIE
CORE
POWER
ISOLATED CORE I/O
PCIE_PVDD
0.1A
1D8V_VGA_S0
0D95V_VGA_S0
2.5A
13mA
25mA
3D3V_VGA_S0
AMD ORB 10U x 1
1U x 6
LF145M 10U x 1
1U x 6
AMD ORB 10U x 6
2.2U x 16
LF145M 4.7U x 6
1U x 20
VGA_CORE
NC on JET
AB13 U10 W9 Y9 W10 T10 AC14 AB12 AB11 AC11 AC13
1.4A
5A
AMD ORB 10U x 2
1U x 3
0.1U x2
LF145M 4.7U x 2
1U x 3
0.1U x 2
Memory phase lock loop power: Dedicated analogue power in for memory PLLs
MPV18
90mA
Engine phase loop power: Dedicated analogue power pin for engine PLL
SPV18
75mA
Engine phase loop power: Dedicated digital power pin for engine PLL
SPV10
100mA
Do Not Stuff
OPS
Iris SKL UMA
Wistron Corporation
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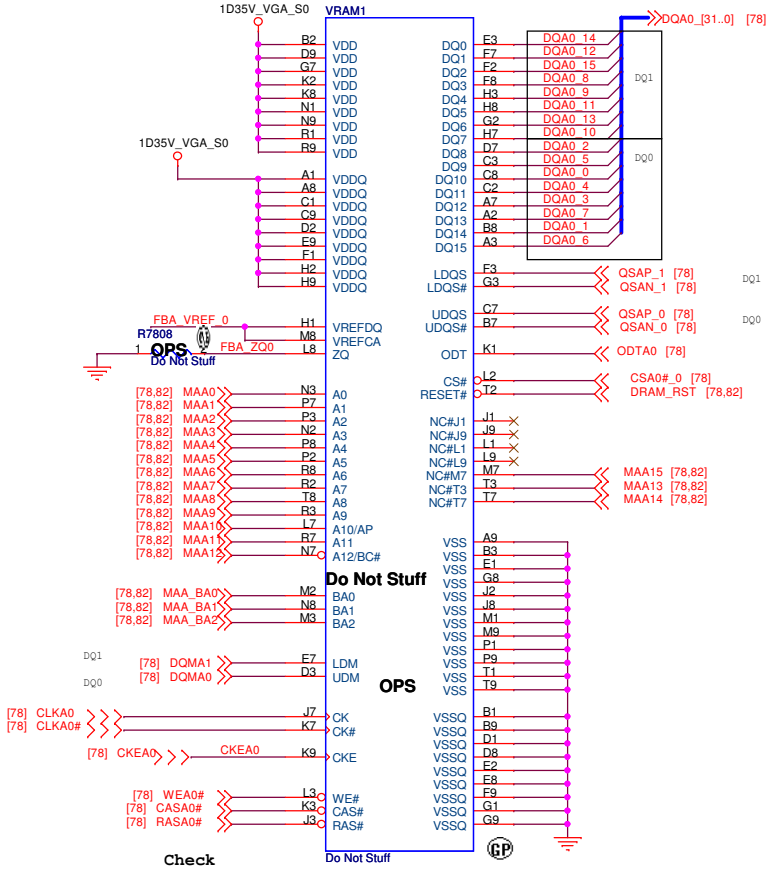
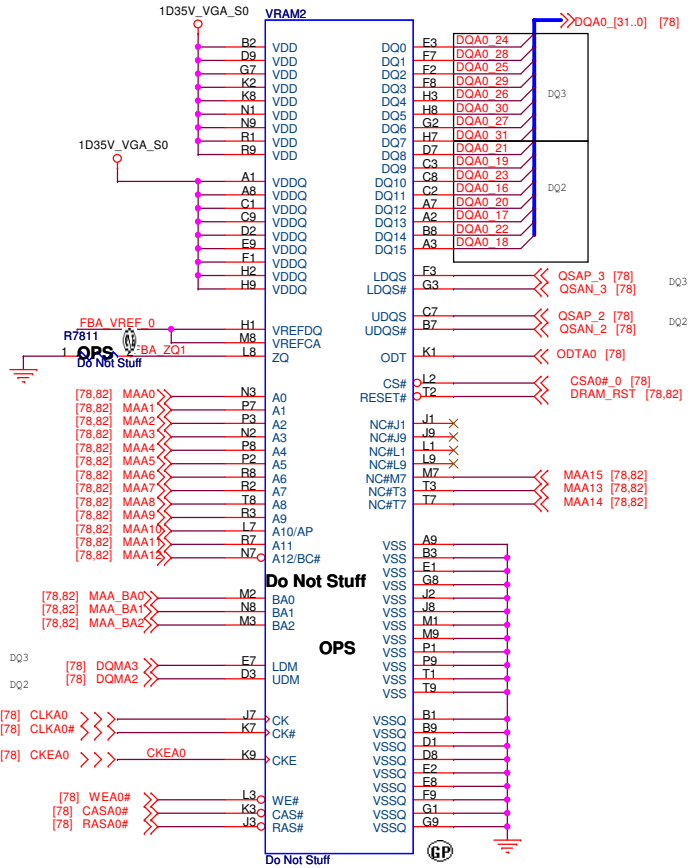
Taipei Hsien 221, Taiwan, R.O.C.
Title
080_GPU (5/5) PWR/GND
Size
Project Name
<Project Name>
Rev
SA
Date: Tuesday, May 26, 2015
Sheet 80 of 105

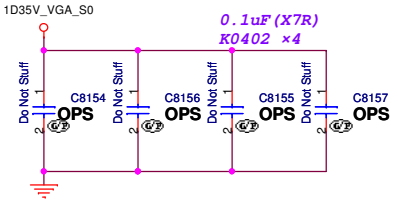
Main Func = dGPU

Data Bits 31:0 RANK 0

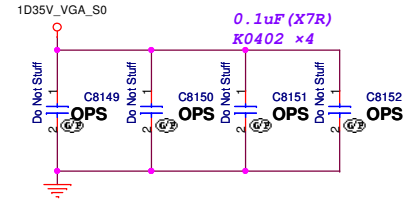




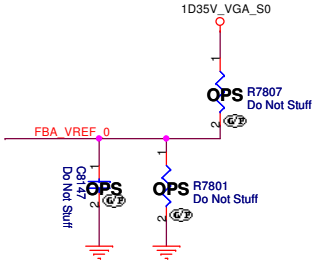
Place close VRAM2 VDD ball



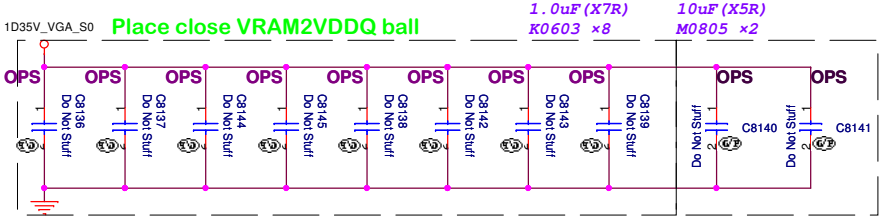
Place close VRAM1VDDQ ball



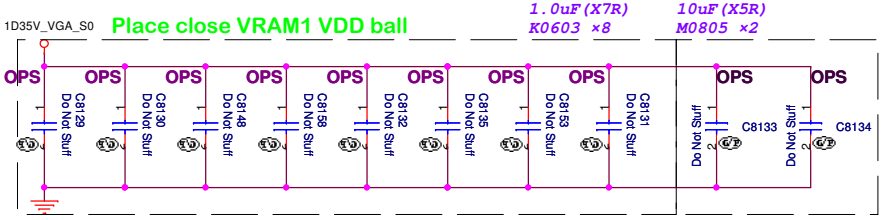
Frame Buffer Patition A-Lower Half



Place close VRAM2VDDQ ball

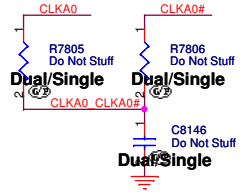


Place close VRAM1 VDD ball



R7805 R7810

Single Rank, 40.2 Ohm = 64.40R25.6DL
Dual Rank, 80.6 Ohm = 64.80R65.6DL



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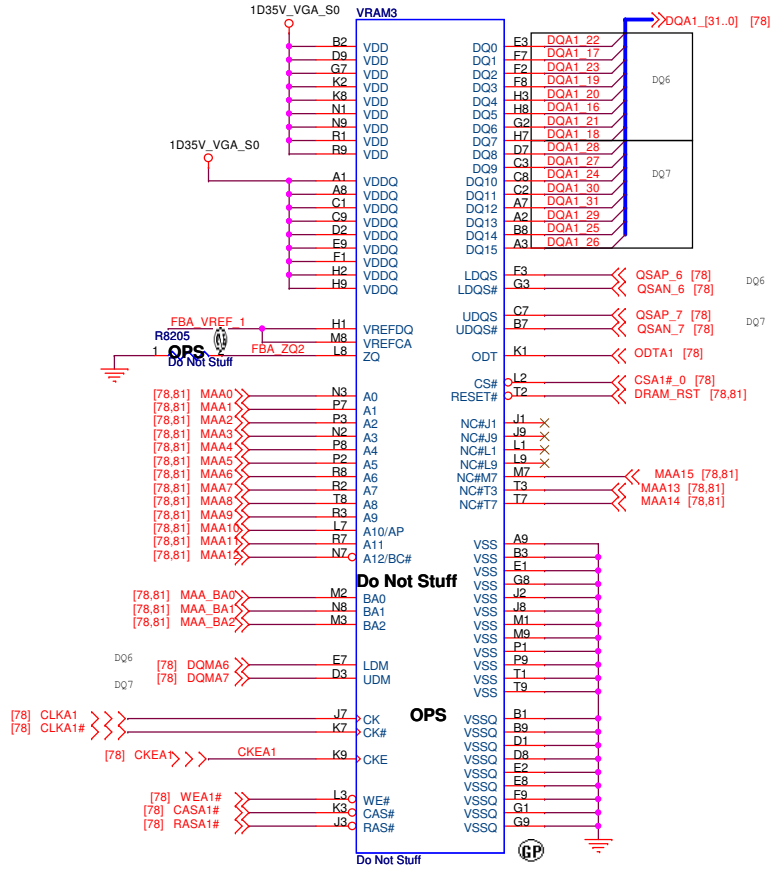
Title: GPU-VRAM1,2 (1/4)

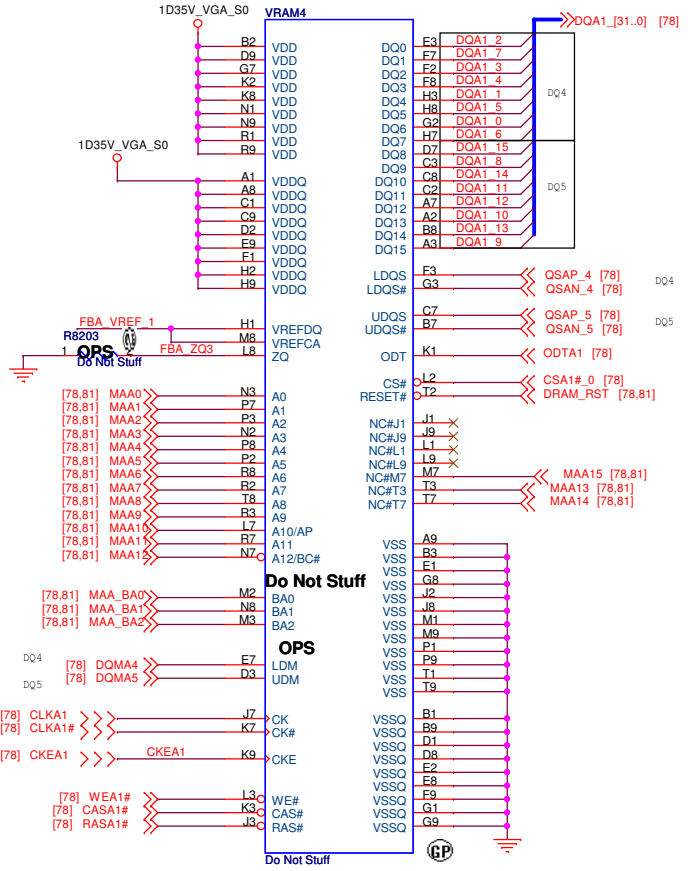
Size	Document Number	Rev
A3	Iris2 SKL-U	A00

Date: Wednesday, September 09, 2015 Sheet 81 of 105

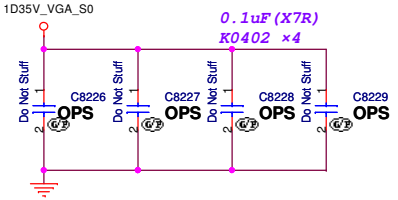
Main Func = dGPU

Data Bits 63:32 RANK 0

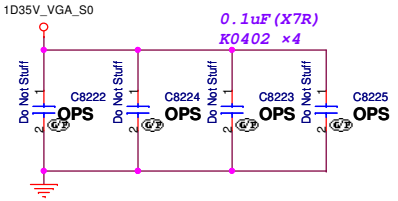




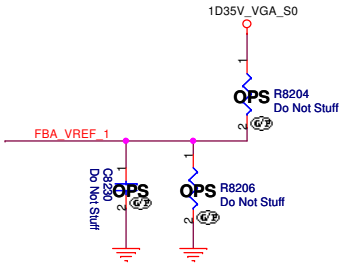
Place close VRAM1VDDQ ball

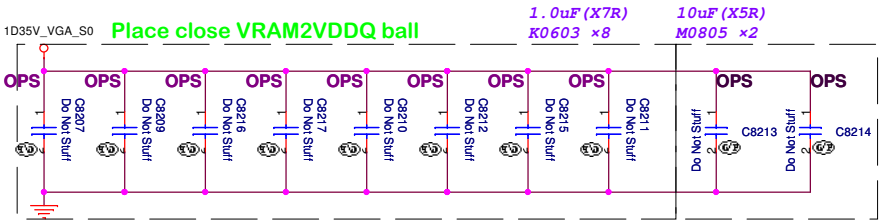


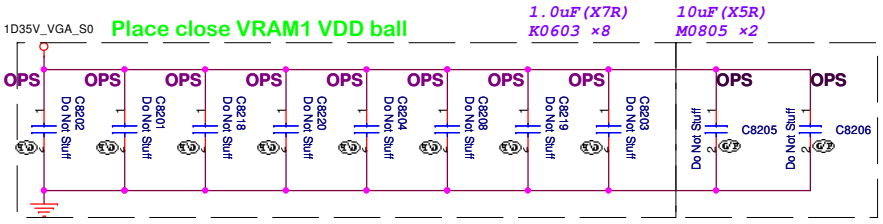
Place close VRAM1VDDQ ball



Frame Buffer Patition A-Lower Half

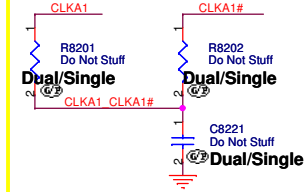






R7905 R7910

Single Rank, 40.2 Ohm
Dual Rank, 80.6 Ohm



Iris SKL UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: A3 | Document Number: Iris2 SKL-U | Rev: A00

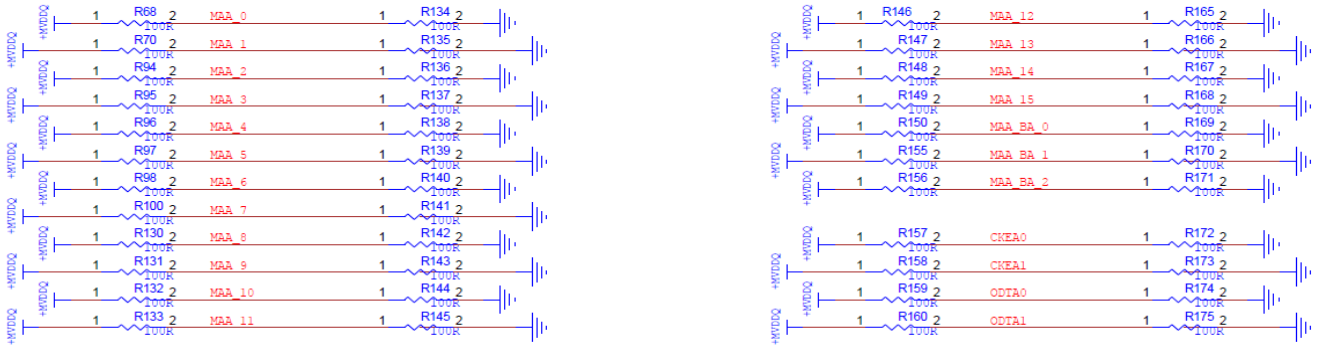
Date: Wednesday, September 09, 2015 | Sheet 82 of 105

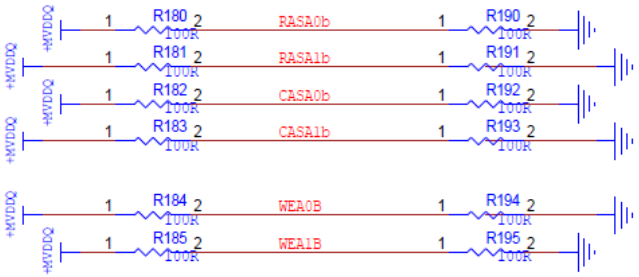
Main Func = dGPU

Data Bits 31:0 RANK 1

Note : Dual Rank need add

For DUAL RANK configuration,
termination might be required based on simulation results
the actual termination value should be OPTIMIZED by the simualtion





Iris SKL UMA

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Title: *GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
A3	Iris2 SKL-U	A00

Date: Tuesday, May 26, 2015 Sheet 83 of 105

Main Func = dGPU

Data Bits 63:32 RANK 1

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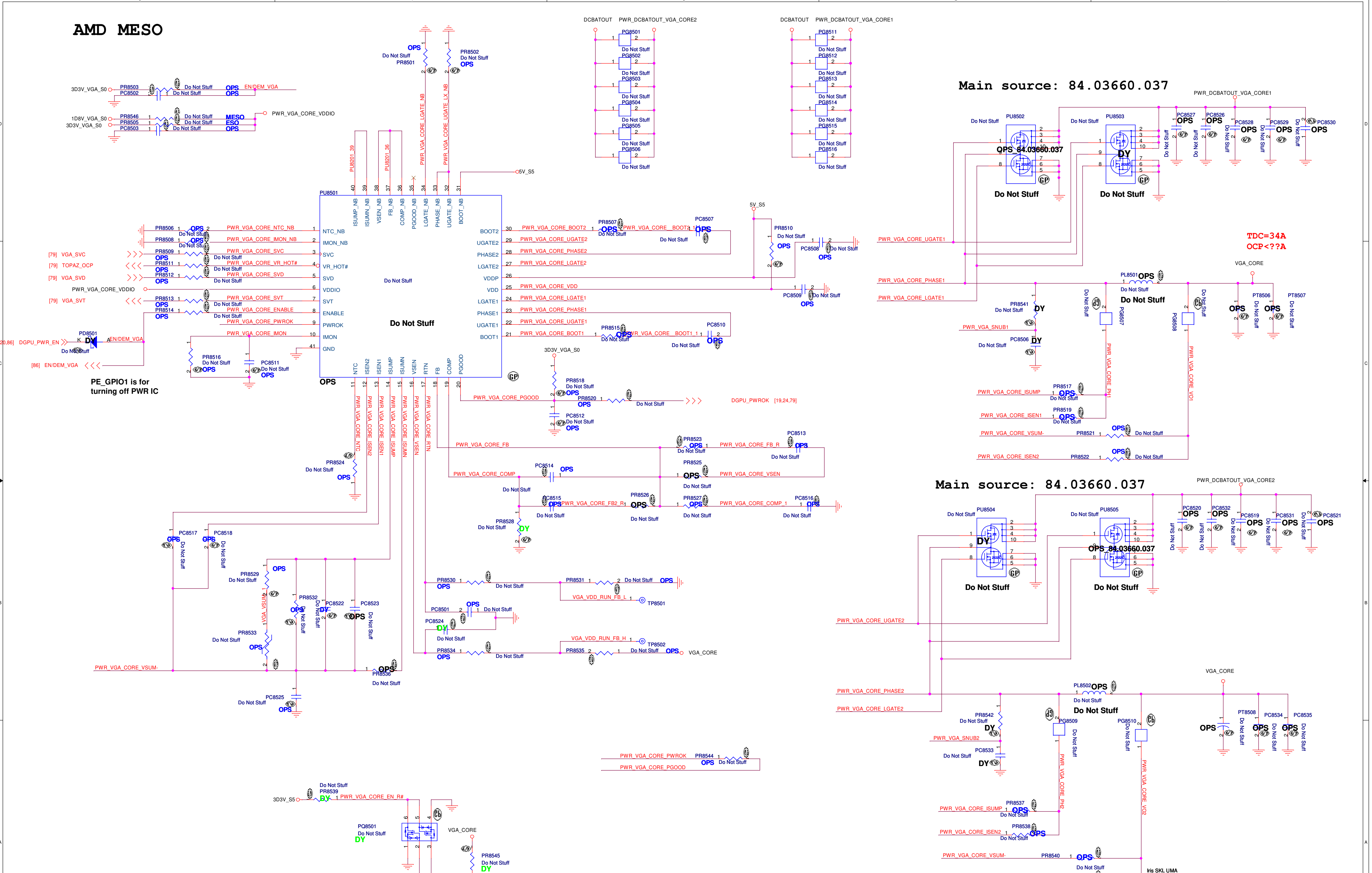
Title: *GPU-VRAM7,8 (4/4)*

Size	Document Number	Rev
A3	Iris2 SKL-U	A00

Date: Tuesday, May 26, 2015 Sheet 84 of 105

AMD MESO



Iris SKL UMA

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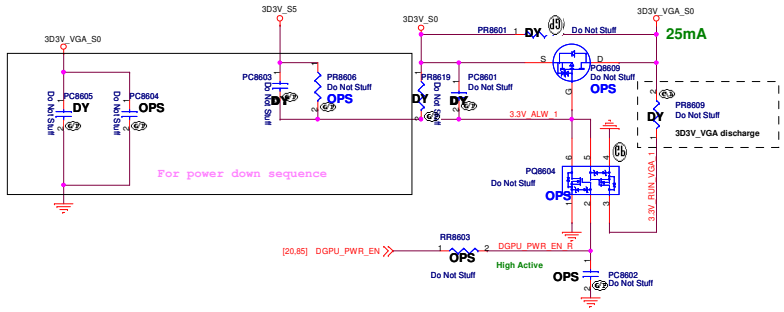
Title

Size: A2 | Document Number | Rev: A00

Date: Wednesday, September 09, 2015 | Sheet 85 of 105

Main Func = dGPU

3D3V_S0 to 3D3V_VGA_S0 Transfer



GPU PWR Sequencing
3D3V_VGAS0

=> 0D95V_VGA_S0/1D8V_VGA_S0

=> 1D35V_VGA_S0

=> VGA_CORE

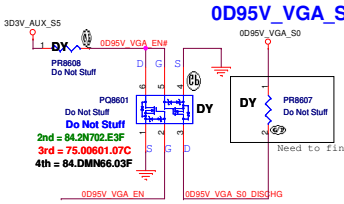
All the ASIC supplies must reach their respective nominal voltages withing 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

It is recommended that the 3.3V rail ramp up first.

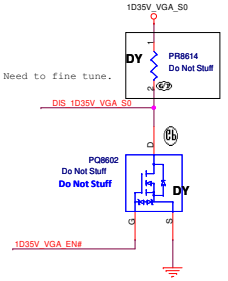
It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.

dGPU Power Discharge Circuit

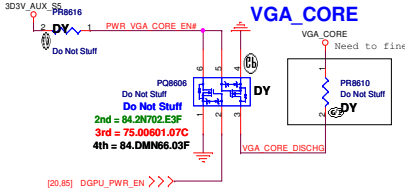
0D95V_VGA_S0



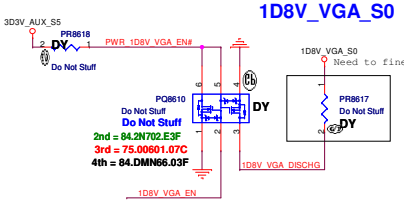
1D35V_VGA_S0



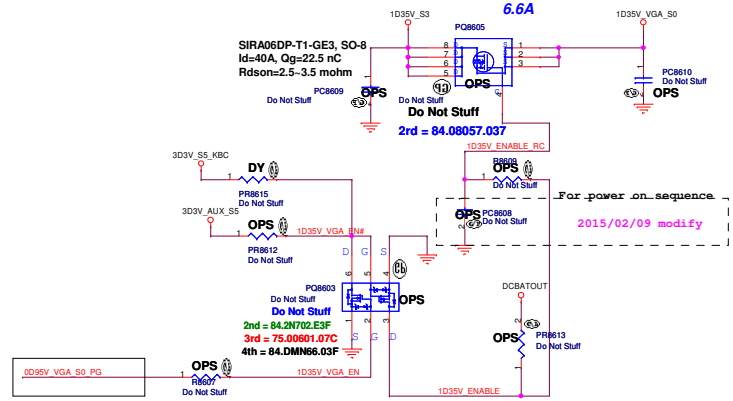
VGA_CORE



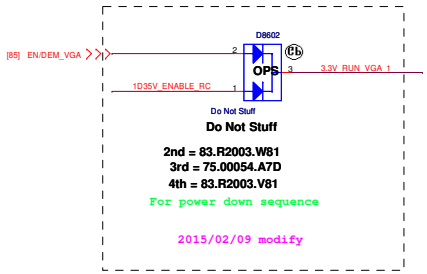
1D8V_VGA_S0



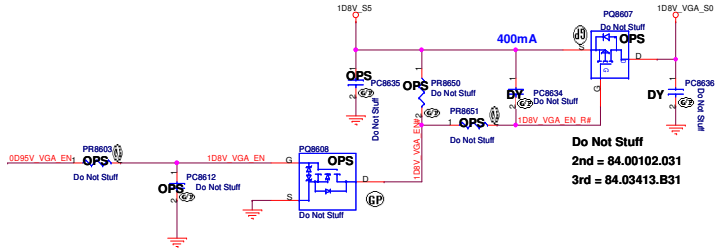
1D35V_VGA_S0



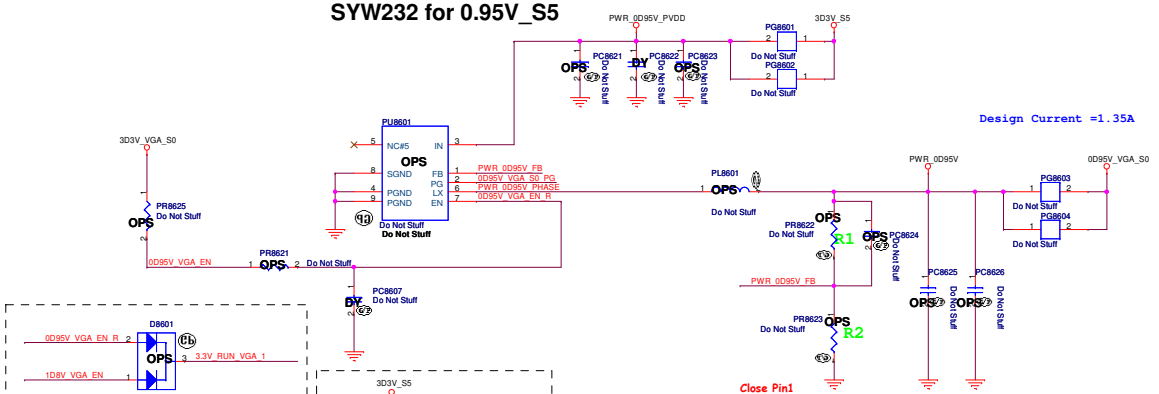
[DG-07158-001 Rev03]

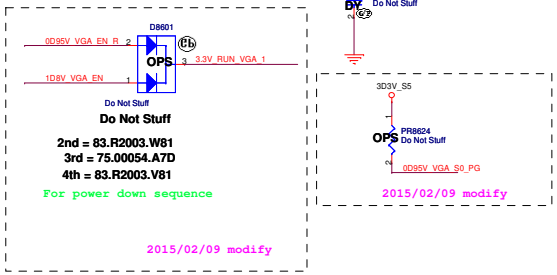


1D8V_VGA_S0



SYW232 for 0.95V_S5





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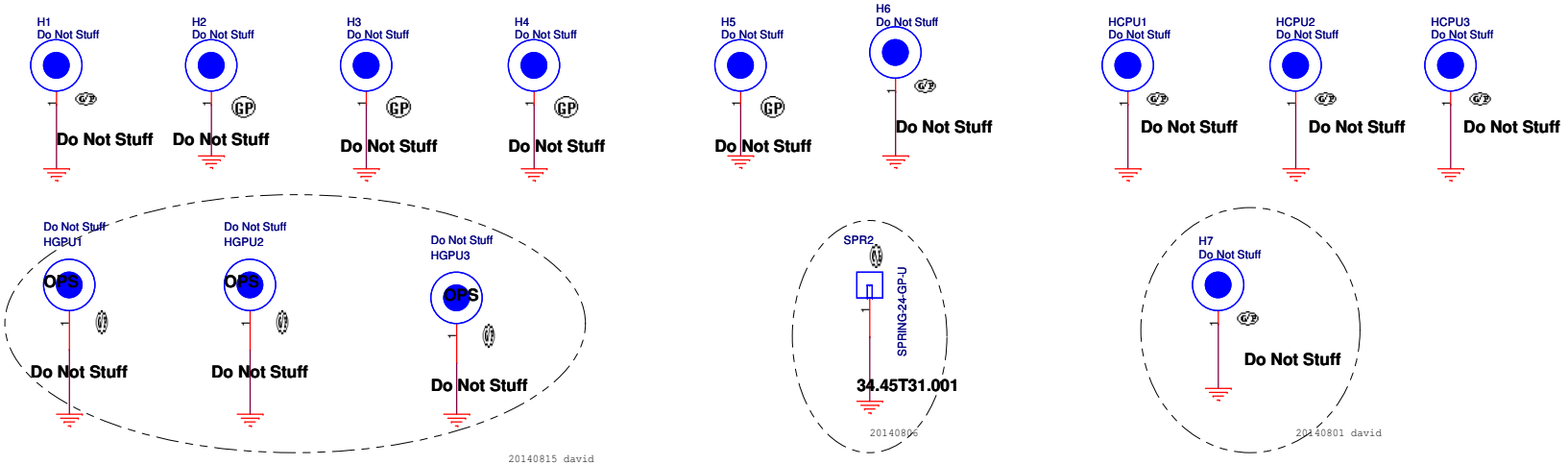
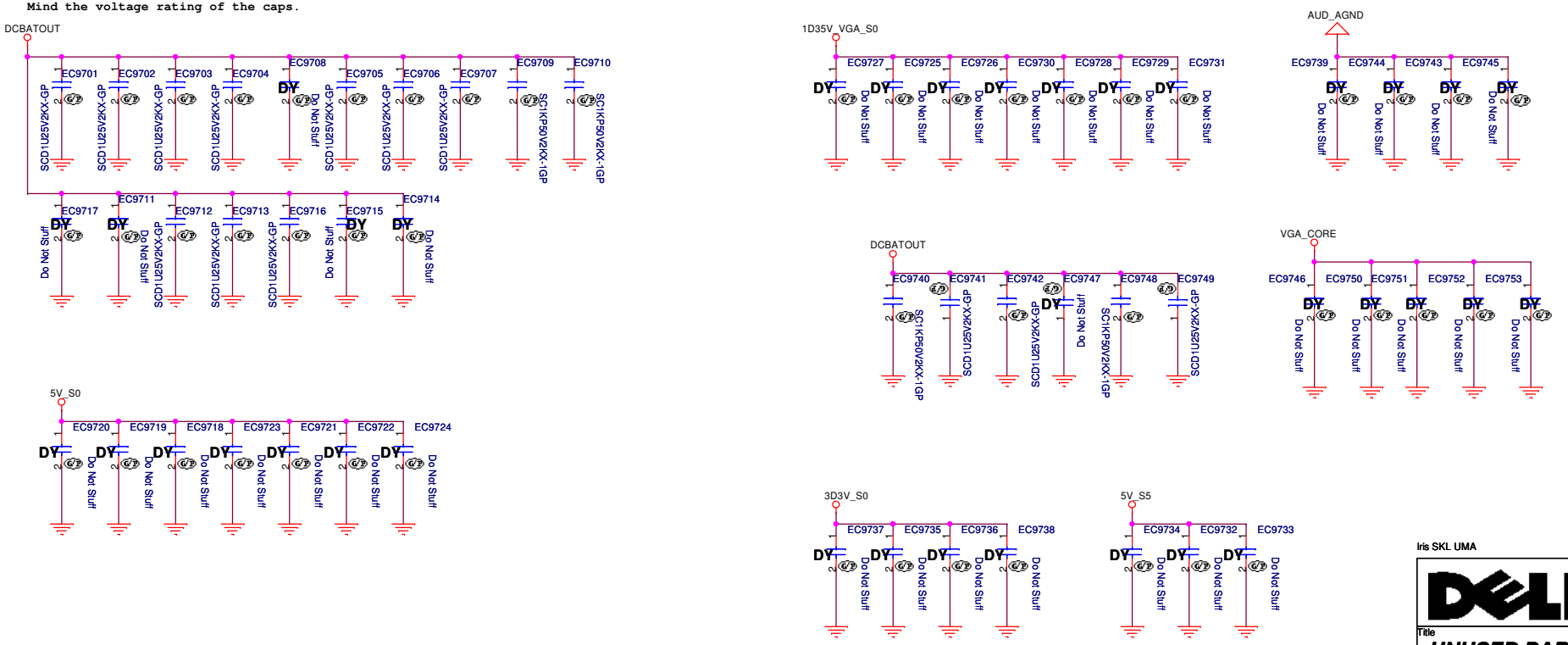
Main Func = UnusedParts



Main Func = EMICapacitors

Mind the voltage rating of the caps.



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Title: *UNUSED PARTS/EMI Capacitors*

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Main Func = Debug

CPU XDP

Layout Note:
ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG<0>

CFG0 — R9908 — FIVR_EN_R
XDP — Do Not Stuff

Layout Note:
ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG<3>

CFG3 — R9902 — XDP_PRSNT_PIN1
XDP — Do Not Stuff

[17] PM_RSMRST# — R9904 — XDP — Do Not Stuff — PM_RSMRST_PWRGD_XDP

[17,24] SIO_PWRBTN# — R9926 — XDP — Do Not Stuff — BP_PWRGD_RST# — C9901 — XDP — Do Not Stuff

SPI0_MOSI_XDP_R — C9903 — XDP — Do Not Stuff

3D3V_S5 — R9909 — XDP — Do Not Stuff

[18] SPI0_MOSI_XDP — R9910 — XDP — Do Not Stuff

[12,13,18,56,65] PCH_SMBDATA — R9911 — XDP — Do Not Stuff — XDP_SMBDAT
[12,13,18,56,65] PCH_SMBCLK — R9912 — XDP — Do Not Stuff — XDP_SMBCLK

[18] PCIE_CLK_XDP_P — R9913 — XDP — Do Not Stuff — PEG_CLK_XDP
[18] PCIE_CLK_XDP_N — R9923 — XDP — Do Not Stuff — PEG_CLK_XDP#

[6] CFG[19:0] — CFG[19:0]
[4] XDP_BPM[3:0] — XDP_BPM[3:0]

XDP_BPM2 — TP9901 Do Not Stuff
XDP_BPM3 — TP9902 Do Not Stuff

+VCCIO — R9906 — XDP — Do Not Stuff — FIVR_EN_R

XDP_PRSNT_PIN1

[16] XDP_PREQ#
[16] XDP_PRDY# — XDP_PRDY#

XDP1 — NP1 / NP2 — XDP — Do Not Stuff

CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7
CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17 CFG18 CFG19

XDP_BPM0 XDP_BPM1
PM_RSMRST_PWRGD_XDP
BP_PWRGD_RST#
FIVR_EN_R
SPI0_MOSI_XDP_R
XDP_SMBDAT
XDP_SMBCLK
XDP_TCLK1

PEG_CLK_XDP
PEG_CLK_XDP#
TP_PMODE_XDP_RST_R_N
XDP_DBRESET#_XDP#
PCH_JTAG_TDO

[4] XDP_TCLK
XDP_TRST# [4]
XDP_TDI [4]
XDP_TMS [4]
XDP_SPI0_IO2 [18]

1D0V_S5

(#543016)Routing of this signal to CFG[0] is OPTIONAL.

PLACE THIS NEAR CPU XDP CONNECTOR

C9905 — XDP — Do Not Stuff

R9925 — XDP — Do Not Stuff — XDP_DBRESET# [17]

EE Note:
Use ZZ.00PAD.Q81 DUMMY PAD for MP.

3D3V_S5 — R9929 — DY — Do Not Stuff
XDP_SPI0_IO2 — R9931 — DY — Do Not Stuff

(#544669)

XDP_TCLK1 — R9914 — DY — Do Not Stuff — PCH_JTAG_TCK [4]
XDP_TCLK — R9915 — DY — Do Not Stuff — XDP_TCK_JTAGX [4]
[4] XDP_TDO_CPU — R9919 — XDP — Do Not Stuff — PCH_JTAG_TDO [4]
XDP_TDI — R9916 — DY — Do Not Stuff — PCH_JTAG_TDI [4]
XDP_TMS — R9917 — DY — Do Not Stuff — PCH_JTAG_TMS [4]

1D0V_S5 — R9927 — XDP — Do Not Stuff — +V1.00A_XDP
+V1.00A_XDP — C9902 — DY — Do Not Stuff
+V1.00A_XDP — C9904 — DY — Do Not Stuff

+V1.00A_XDP — R9932 — XDP — Do Not Stuff
[6] ITP_PMODE — R9933 — XDP — Do Not Stuff — TP_PMODE_XDP_RST_R_N

(#544669 Rev0.52) NC.

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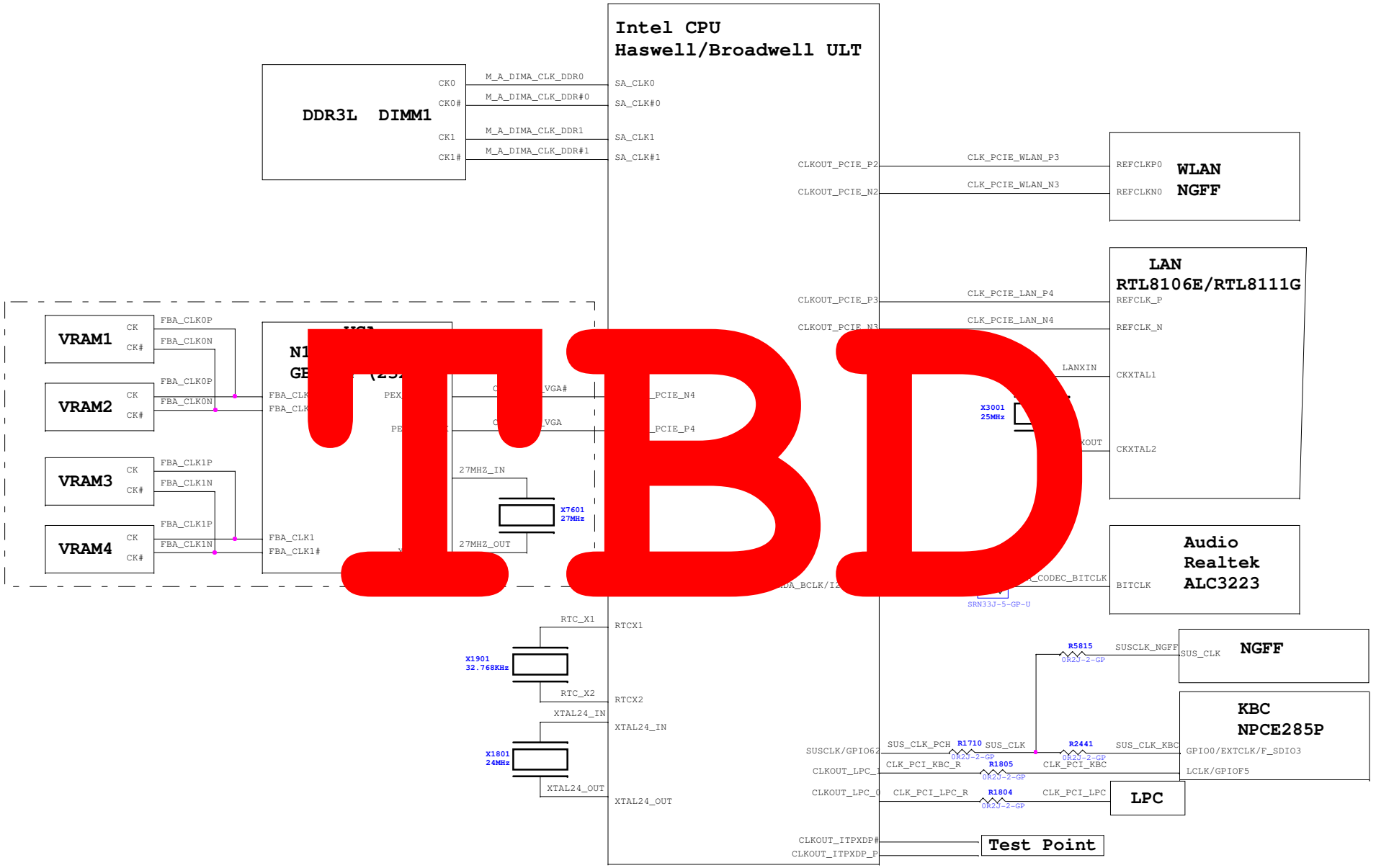
CLK Block Diagram



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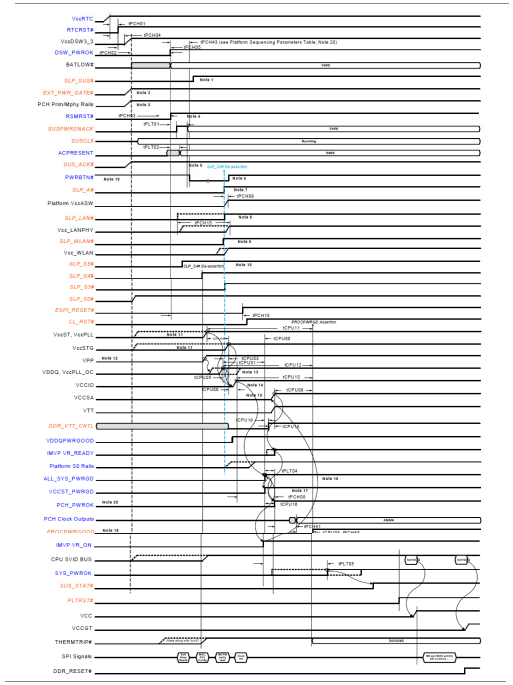
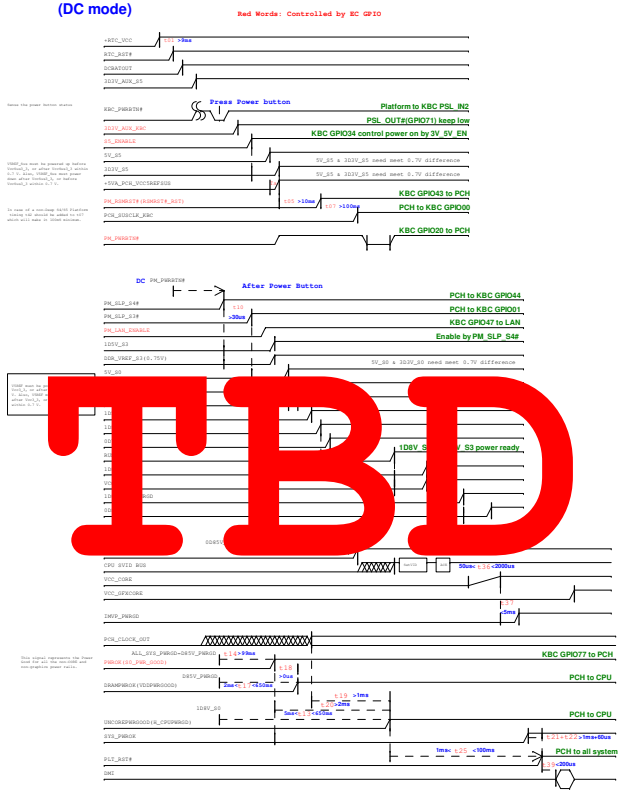
SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]

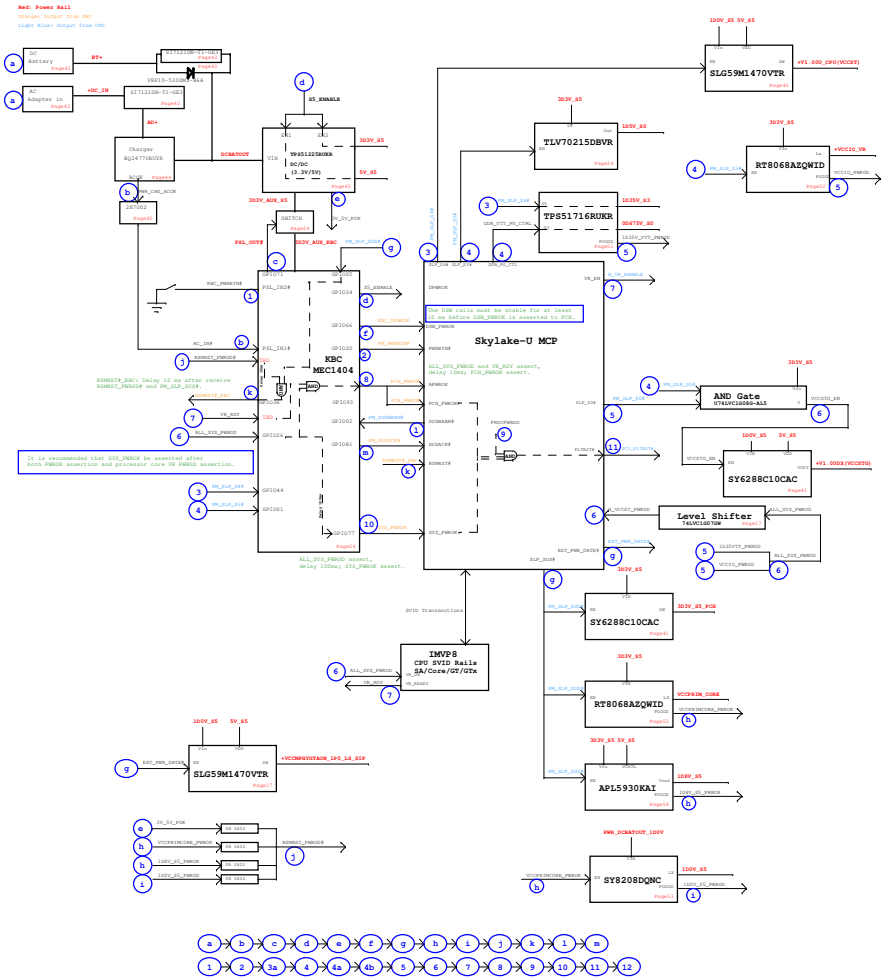


(DC mode)

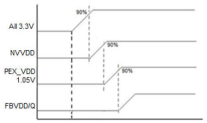


TBD

Tulip Skylake POWER UP SEQUENCE DIAGRAM (Deep Sx Platform)



[dGPU] N16x Power-Up/Down Sequence



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Note:
- The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- The previous power rail must ramp up to 90% before the next power rail can start ramping up.
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.
- The order of NVVDD and PEX_VDD ramp-up can be reversed during GC6 exit when there is a back-to-back GC6 entry/exit and/or when PEX_VDD takes longer to ramp down during GC6 entry.

3.10.2.2 Power-Down Sequence

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

[dGPU] GC6 2.0 Power-Up/Down Sequence

18.3.2.3 GC6 2.0 Entry/Exit Timing

The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0 en and exit sequence and timing requirements.

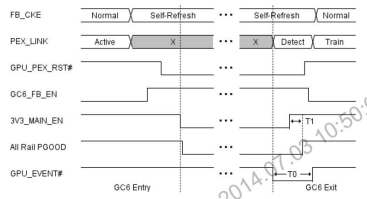


Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-2. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:
- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

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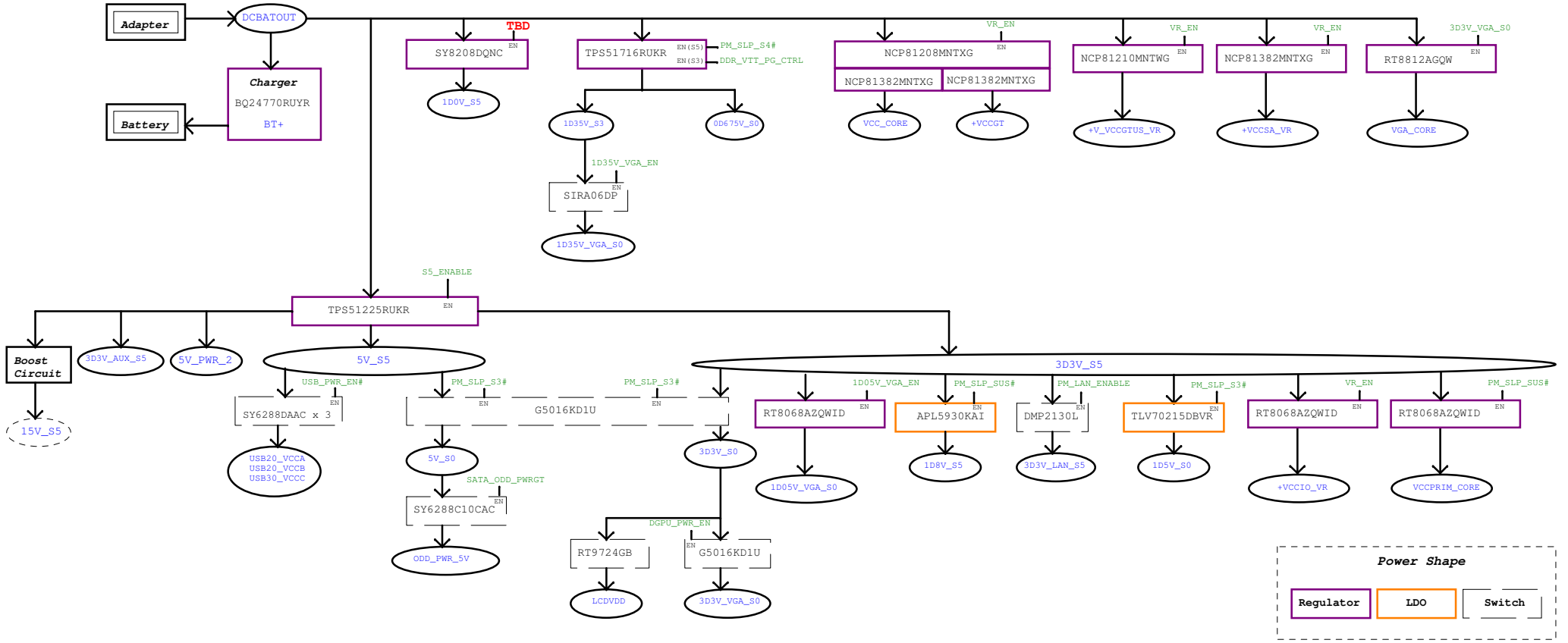
Power Sequence

Wis SKL-U



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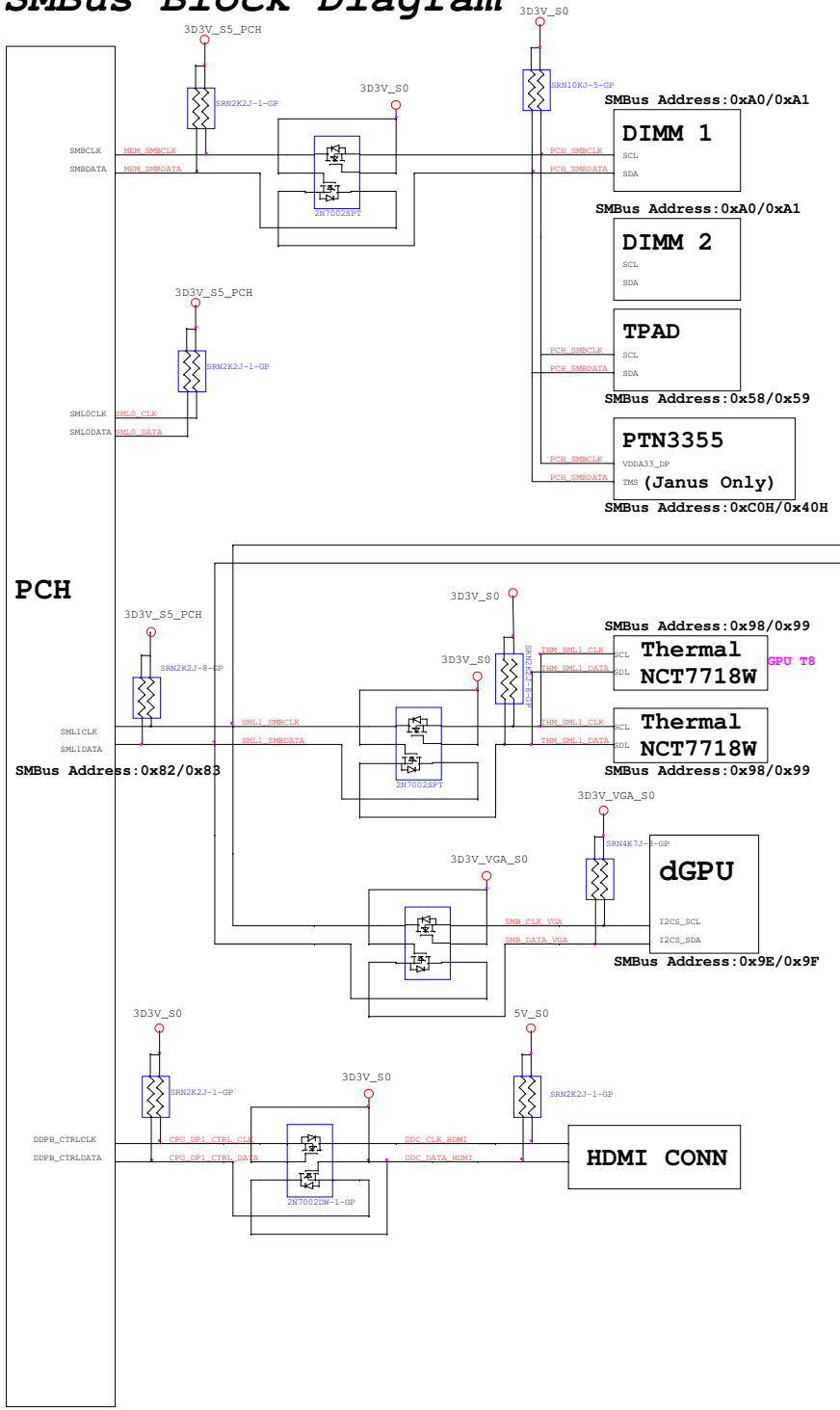
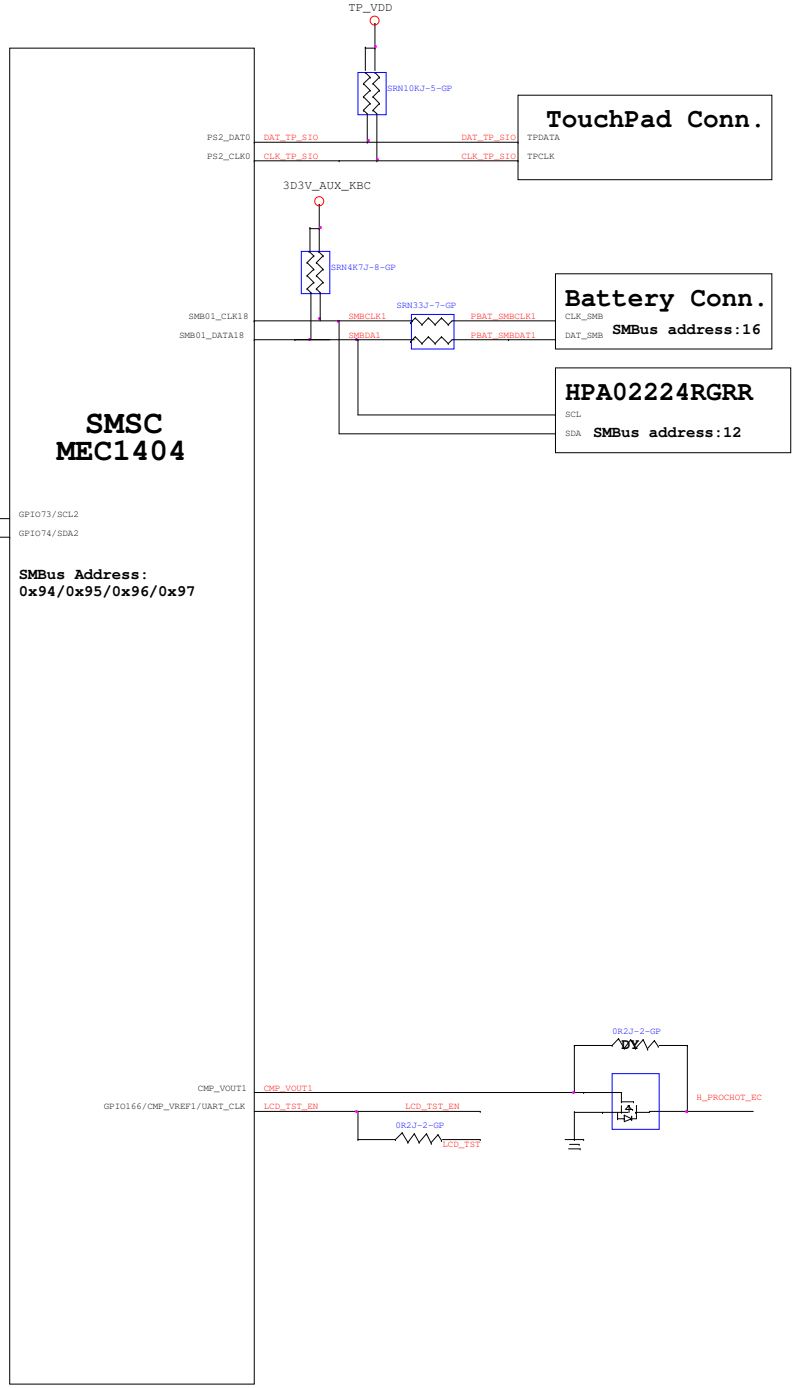
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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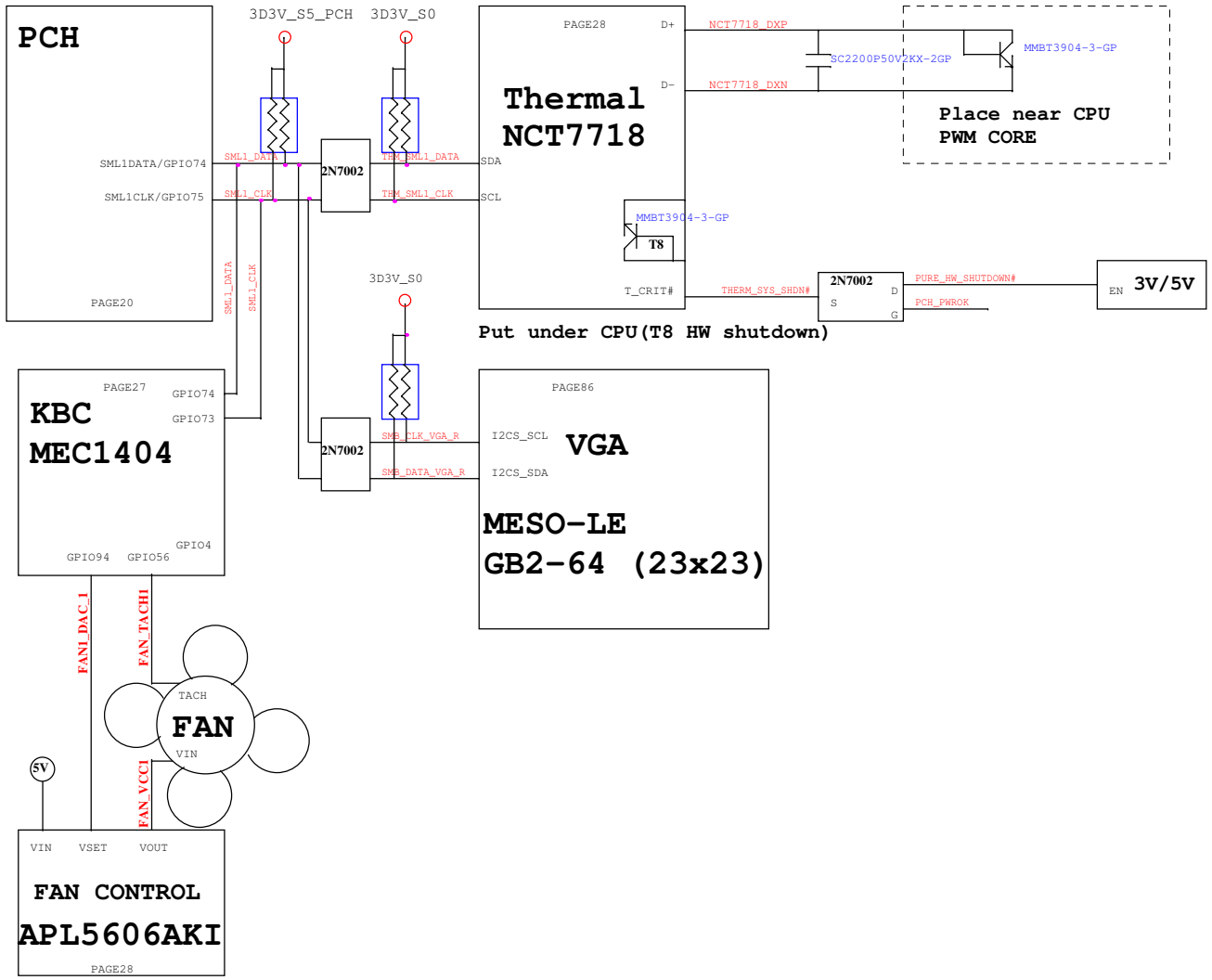
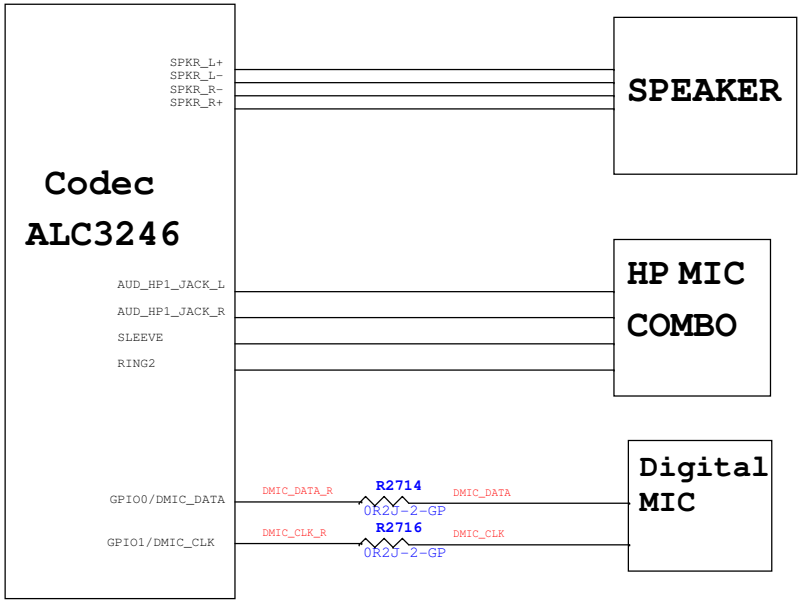
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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